

## Synchronous Step-Down DC/DC Controller IC - Input Voltage : 25V

☆GreenOperation Compatible

### ■GENERAL DESCRIPTION

The XC9213 series is N-ch & N-ch drive, synchronous, step-down DC/DC controller IC with a built-in bootstrap driver circuit. Output will be stable no matter which load capacitors, including low ESR capacitors, are used.

Resistance ( $R_{SENSE}$ ) of about several  $10m\Omega$  will be required as a current sense. The phase compensation is also run when a low ESR capacitor is used. In addition, the circuit is double protected by the ways of limiting the current while detecting overshoot current and making output shutdown at any given timing by a protection time setting capacitor (CPRO).

The output voltage can be set freely within a range of 1.5V~15.0V with 1.0V (accuracy  $\pm 2\%$ ) of internal reference voltage by using externally connected resistors (RFB1, 2). Synchronous rectification PWM control can be switched to non-synchronous current limit PFM/PWM automatic switchable control (=voltage between  $R_{SENSE}$  pins) by using the MODE pin.

The series has a built-in voltage detector for monitoring a selected voltage by external resistors.

During stand-by (CE pin = low) all circuits are shutdown to reduce current consumption to as low as  $4.0\mu A$  or less.

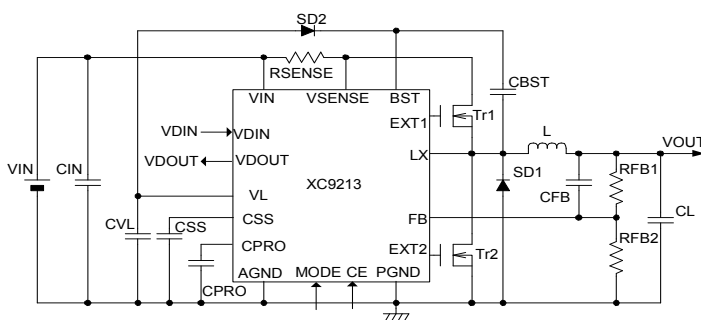
### ■APPLICATIONS

- PDAs
- Mobile phones
- Note book computers
- Portable audio systems
- Various multi-function power supplies

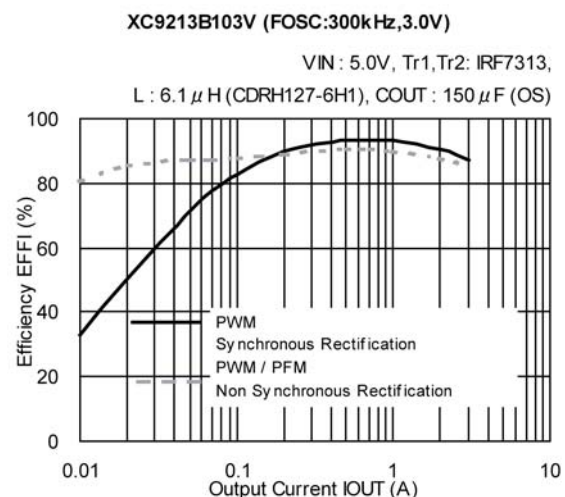
### ■FEATURES

<b>Input Voltage Range</b>	: 4.0V ~ 25.0V
<b>Output Voltage Range</b>	: 1.5V ~ 15.0V externally set
<b>Reference voltage</b>	: 1.0V ( $\pm 2\%$ )
<b>Oscillation Frequency</b>	: 300kHz ( $\pm 15\%$ )
<b>Output Current</b>	: 5A ( $V_{IN}=5.0V, V_{OUT}=3.3V$ )
<b>Control</b>	: PWM/PFM manual control
<b>Current Limit Protection</b>	: Sense Voltage=170mV
<b>High Efficiency</b>	: 93% ( $V_{IN}=5.0V, V_{OUT}=3.3V, I_{OUT}=1A$ )
<b>Detect Voltage Function</b>	: Detects 0.9V/Open-drain output
<b>Stand-by Current</b>	: $I_{STB} = 4.0\mu A$ (MAX.)
<b>Load Capacitor</b>	: Low ESR capacitor
<b>Shutdown Time</b>	: Adjustable by CPRO pin
<b>Built-in Bootstrap</b>	: External Nch-Nch Drivers
<b>Package</b>	: TSSOP-16
<b>Environmentally friendly</b>	: EU RoHS Compliant, Pb Free

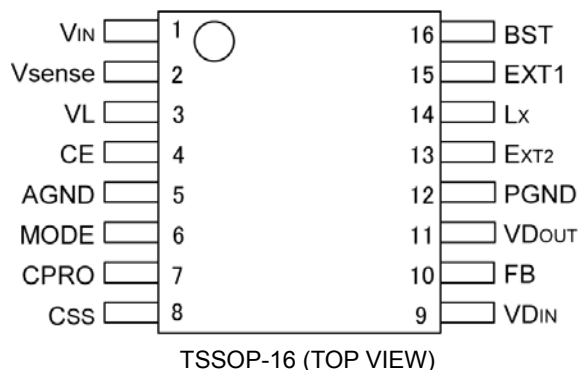
### ■TYPICAL APPLICATION CIRCUIT



### ■TYPICAL PERFORMANCE CHARACTERISTICS



## PIN CONFIGURATION



## PIN ASSIGNMENT

PIN NUMBER	PIN NAME	FUNCTION
1	VIN	Input Voltage
2	VSENSE	Current Detection
3	VL	Local Power Supply
4	CE	Chip Enable
5	AGND	Analog Ground
6	MODE	PWM / Current Limit PFM Switch
7	CPRO	Protection Time Setting Capacitor Connection <Set shutdown time of VOUT when detecting overcurrent>
8	CSS	Soft-start Capacitor Connection <Set soft-start time>
9	VDIN	Voltage Detector Input (0.9V)
10	FB	Output Voltage Setting Resistor Connection < Set output voltage freely by split resistors >
11	VDOUT	Voltage Detector Output (Open-Drain)
12	PGND	Power Ground
13	EXT2	Low Side N-ch Driver Transistor <Connect to Gate of Low Side N-ch MOSFET >
14	LX	Coil Connection
15	EXT1	High Side N-ch Driver Transistor <Connect to Gate of High Side N-ch MOSFET >
16	BST	Bootstrap

## CE PIN & MODE PIN FUNCTION

CE PIN	OPERATIONAL STATE
H	Operation
L	Shut down

MODE PIN	OPERATIONAL STATE
H	Synchronous
	PWM Control
L	Non-Synchronous
	PWM / Current Limit PFM Automatic Switching Control

## PRODUCT CLASSIFICATION

### Ordering Information

XC9213B①②③④⑤-⑥<sup>(\*)</sup>

DESIGNATOR	DESCRIPTION	SYMBOL	DESCRIPTION
①②	Reference Voltage	10	1.0V (Fixed)
③	Oscillation Frequency	3	300kHz
④⑤-⑥	Package (Order Unit)	VR	TSSOP-16 (3,000/Reel)
		VR-G	TSSOP-16 (3,000/Reel)

<sup>(\*)</sup> The "-G" suffix indicates that the products are Halogen and Antimony free as well as being fully RoHS compliant.

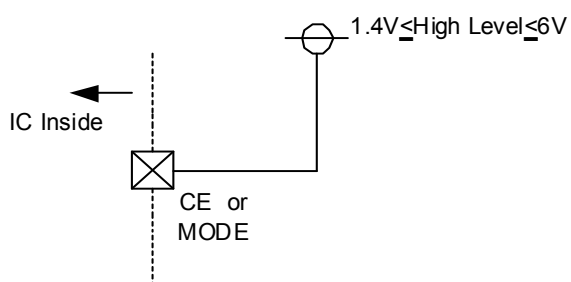
## ■ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNITS
V <sub>IN</sub> Pin Voltage	V <sub>IN</sub>	- 0.3 ~ 30.0	V
V <sub>SENSE</sub> Pin Voltage	V <sub>SENSE</sub>	- 0.3 ~ 30.0	V
V <sub>L</sub> Pin Voltage	V <sub>L</sub>	- 0.3 ~ 6.0	V
CE Pin Voltage (*)	CE	- 0.3 ~ 30.0	V
MODE Pin Voltage (*)	MODE	- 0.3 ~ 30.0	V
C <sub>PRO</sub> Pin Voltage	C <sub>PRO</sub>	- 0.3 ~ 6.0	V
C <sub>SS</sub> Pin Voltage	C <sub>SS</sub>	- 0.3 ~ 6.0	V
V <sub>DIN</sub> Pin Voltage	V <sub>DIN</sub>	- 0.3 ~ 6.0	V
FB Pin Voltage	FB	- 0.3 ~ 6.0	V
V <sub>DOUT</sub> Pin Voltage	V <sub>DOUT</sub>	- 0.3 ~ 30.0	V
EXT2 Pin Voltage	EXT2	- 0.3 ~ 6.0	V
L <sub>x</sub> Pin Voltage	L <sub>x</sub>	- 0.3 ~ 30.0	V
EXT1 Pin Voltage	EXT1	- 0.3 ~ 30.0	V
BST Pin Voltage	BST	- 0.3 ~ 30.0	V
EXT1 Pin Current	I <sub>EXT1</sub>	±100	mA
EXT2 Pin Current	I <sub>EXT2</sub>	±100	mA
L <sub>x</sub> Pin Current	I <sub>Lx</sub>	100	mA
Power Dissipation	P <sub>d</sub>	350	mW
Operational Temperature Range	T <sub>opr</sub>	- 40 ~ + 85	°C
Storage Temperature Range	T <sub>stg</sub>	- 55 ~ + 125	°C

(\*) CE, MODE pin voltage

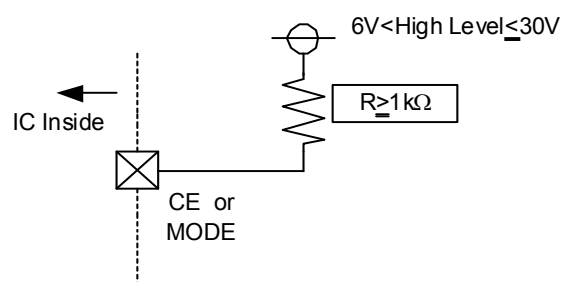
1)  $1.4V \leq \text{High Level} \leq 6V$

The CE pin and the MODE pin can be connected directly to the high level power supply.



2)  $6V < \text{High Level} \leq 30V$

The CE pin and the MODE pin should be connected to over 1kΩ resistor when connecting



## ELECTRICAL CHARACTERISTICS

XC9213B103 (FOSC = 300kHz)

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Input Voltage (*2)	V <sub>IN</sub>		4.0	-	25.0	V	-
Output Voltage Setting Range	V <sub>OUTSET</sub>		1.5	-	15.0	V	-
FB Control Voltage	V <sub>FB</sub>		0.980	1.000	1.020	V	1
U.V.L.O. Voltage	UVLO	Voltage which EXT1 pin starts oscillation	1.0	1.5	2.0	V	2
Supply Current 1	I <sub>DD1</sub>	CE=V <sub>IN</sub> , FB=0.9V	-	550	800	μA	3
Supply Current 2	I <sub>DD2</sub>	CE=V <sub>IN</sub> , FB=1.1V	-	450	600	μA	3
Stand-by Current	I <sub>STB</sub>	CE=FB=0V	-	-	4.0	μA	4
Oscillation Frequency	FOSC	CE=V <sub>IN</sub> , FB=0.9V	255	300	345	kHz	5
Maximum Duty Ratio 1	MAXDTY1	CE=V <sub>IN</sub> , FB=0.9V	91	95	-	%	5
Maximum Duty Ratio 2	MAXDTY2	CE=V <sub>IN</sub> , FB=1.1V	-	98	-	%	5
PFM Duty Ratio	PFMDTY	With external components, V <sub>OUT</sub> =3V, MODE=0V, I <sub>OUT</sub> =1mA, No R <sub>SENSE</sub>	2.5	3.0	3.9	μs	6
Sense Voltage	V <sub>SENSE</sub>	Voltage which EXT1 pin stops oscillation	145	170	200	mV	7
CPRO time	T <sub>PRO</sub>	C <sub>PRO</sub> =4700pF, V <sub>SENSE</sub> =0V→0.5V, Time until V <sub>DOUT</sub> inverts H to L	2.3	4.7	9.4	ms	8
Soft-Start Time	T <sub>SS</sub>	With external components, C <sub>SS</sub> =4700pF, CE=0V→3V, Time until voltage becomes V <sub>OUT</sub> x 0.95	4	8	21	ms	9
Short Protection Circuit Operating Voltage	V <sub>SHORT</sub>	V <sub>IN</sub> -V <sub>SENSE</sub> : 0.3V fixed, FB: SWEEP. Voltage which V <sub>DOUT</sub> inverts H to L	0.15	0.40	0.72	V	25
Efficiency	EFFI	With external components, I <sub>OUT</sub> =1A, V <sub>OUT</sub> =3.0V	-	93	-	%	10
CE "H" Voltage	V <sub>CEH</sub>	Voltage which EXT1 pin starts oscillation	1.4	-	-	V	11
CE "L" Voltage	V <sub>CEL</sub>	Voltage which EXT1 pin voltage holding "L" level	-	-	0.4	V	11
MODE "H" Voltage	V <sub>MODEH</sub>	Voltage which EXT2 pin starts oscillation	1.4	-	-	V	12
MODE "L" Voltage	V <sub>MODEL</sub>	Voltage which EXT2 pin voltage holding "L" level	-	-	0.4	V	12
EXT1 "H" ON Resistance	R <sub>EXT1H</sub>	FB=0.9V, EXT1=3.6V	-	18	23	Ω	13
EXT1 "L" ON Resistance	R <sub>EXT1L</sub>	FB=1.1V, EXT1=0.4V	-	11	18	Ω	14
EXT2 "H" ON Resistance	R <sub>EXT2H</sub>	FB=1.1V, EXT1=3.6V	-	18	23	Ω	15
EXT2 "L" ON Resistance	R <sub>EXT2L</sub>	FB=0.9V, EXT2=0.4V	-	4	8	Ω	16
Dead Time 1	T <sub>DT1</sub>	With external components, EXT1: H→L, EXT2: L→H	-	100	-	ns	10
Dead Time 2	T <sub>DT2</sub>	With external components, EXT2: H→L, EXT1: L→H	-	60	-	ns	10
CE "H" Current	I <sub>CEH</sub>	CE=5.0V	-	-	0.1	μA	17
CE "L" Current	I <sub>CEL</sub>	CE=0V	-0.1	-	-	μA	17
MODE "H" Current	I <sub>MODEH</sub>	MODE=5.0V	-	-	0.1	μA	18
MODE "L" Current	I <sub>MODEL</sub>	MODE=0V	-0.1	-	-	μA	18
C <sub>SS</sub> Current	I <sub>CSS</sub>	C <sub>SS</sub> =0V	-4.0	-2.0	-	μA	19
FB "H" Current	I <sub>FBH</sub>	FB=5.0V	-	-	0.1	μA	20
FB "L" Current	I <sub>FBL</sub>	FB=0V	-0.1	-	-	μA	20

## ■ ELECTRICAL CHARACTERISTICS (Continued)

XC9213B103 (Continued)

### ● Voltage Regulator (\*3)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Output Voltage	V <sub>LOUT</sub>	FB=1.1V, I <sub>LOUT</sub> =10mA	3.86	4.00	4.14	V	21
Load Regulation	$\Delta V_{LOUT}$	FB=1.1V, 1mA ≤ I <sub>LOUT</sub> ≤ 30mA	-	45	90	mV	21
Input Regulation	$\frac{\Delta V_{LOUT}}{\Delta V_{IN} \cdot V_{LOUT}}$	FB=1.1V, I <sub>LOUT</sub> =10mA, V <sub>LOUT</sub> +1V ≤ V <sub>IN</sub> ≤ 25V	-	0.05	0.1	%/V	21

### ● Voltage Detector

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Detect Voltage	V <sub>DF</sub>	FB=1.1V, Voltage which V <sub>DOUT</sub> inverts H to L	0.855	0.900	0.925	V	22
Release Voltage (*4)	V <sub>DR</sub>	FB=1.1V, Voltage which V <sub>DOUT</sub> inverts L to H	0.915	0.954	0.980	V	22
Hysteresis Range	HYS	FB=1.1V	2.9	6.0	7.5	%	22
Output Current	V <sub>DOUT</sub>	FB=1.1V, V <sub>DIN</sub> =V <sub>DF</sub> -0.4V, V <sub>DOUT</sub> =0.5V	5	15	20	mA	23
Delay Time	TDLY	V <sub>DR</sub> → V <sub>DOUT</sub> inversion	-	-	10	μs	22
V <sub>DIN</sub> Current	I <sub>VDIN</sub>	V <sub>DIN</sub> =5.0V	-	-	0.1	μA	24

NOTE:

\*1: Unless otherwise stated, V<sub>IN</sub>=5.0V, CE=5.0V, MODE=5.0V, FB=0.9V

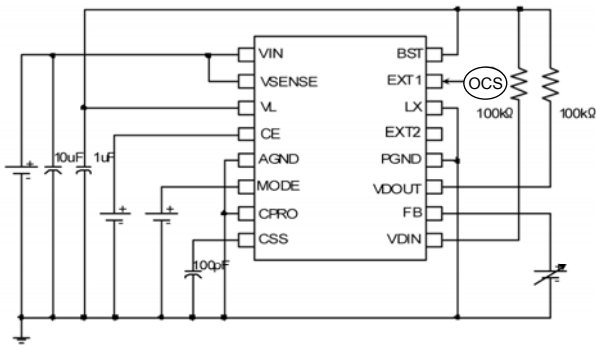
\*2: The operation may not be stable at no load, if the step-down ratio (V<sub>OUT</sub>/V<sub>IN</sub> × 100) becomes lower than 12%.

\*3: The regulator block is used only for bootstrap. Please do not use as a local power supply.

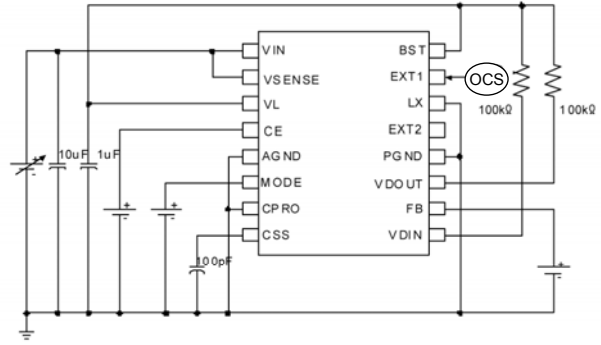
\*4: Release voltage: (V<sub>DR</sub>) = V<sub>DF</sub> + HYS × V<sub>DF</sub>

## TEST CIRCUITS

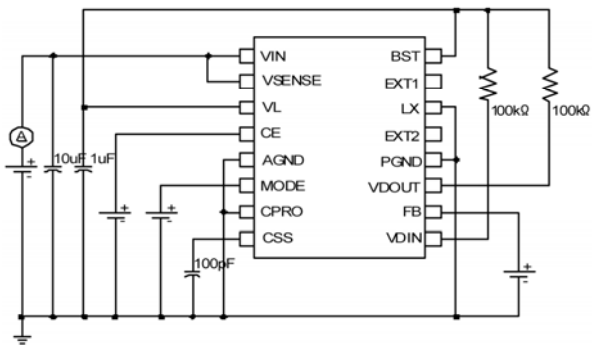
Circuit 1



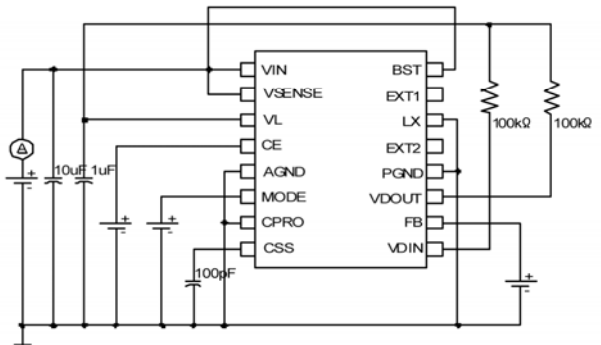
Circuit 2



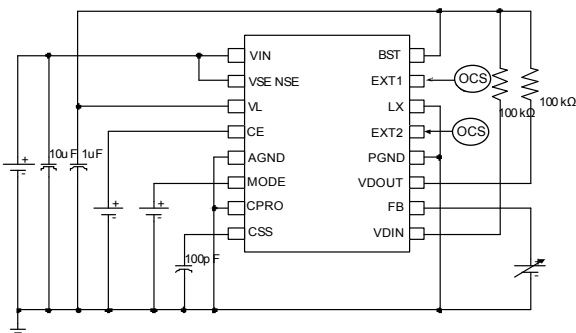
Circuit 3



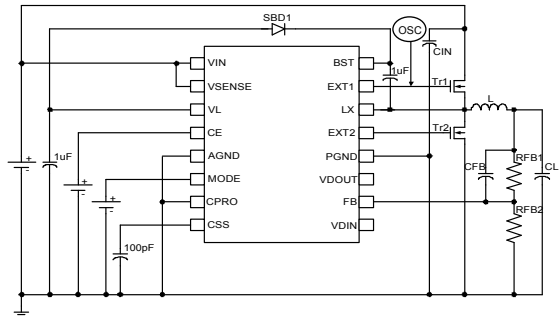
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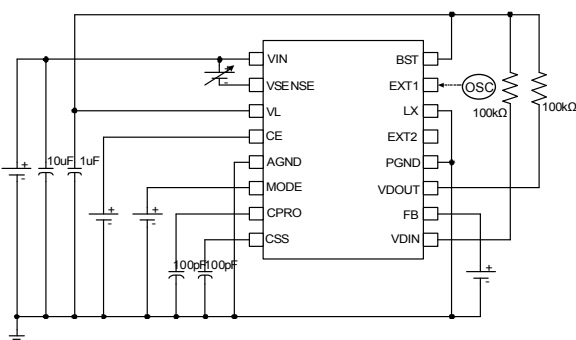
Circuit 5



Circuit 6



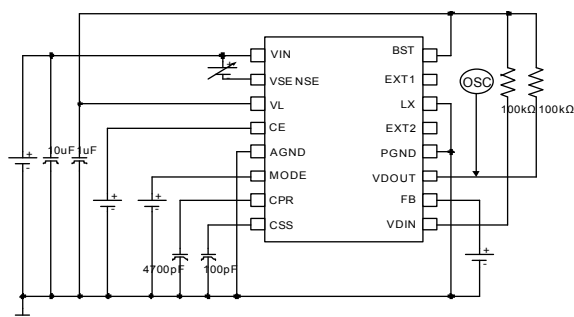
Circuit 7



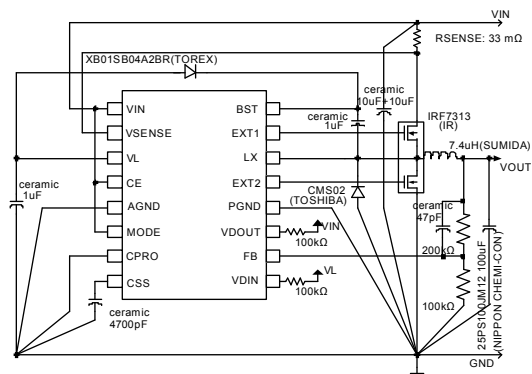
Tr1:	2SK2857 (NEC)
Tr2:	2SK2857 (NEC)
SBD1:	CRS02 (TOSHIBA)
L:	22 $\mu$ H CDRH6D28 (SUMIDA)
CL:	100 $\mu$ F (OS-CON, NIPPON CHEMI-CON)
CIN1:	22 $\mu$ F (OS-CON, SANYO)
RFB1:	220k $\Omega$
RFB2:	110k $\Omega$
CFB:	68pF

## ■ TEST CIRCUITS (Continued)

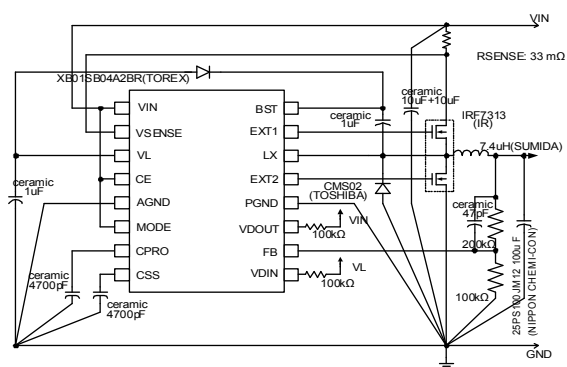
Circuit 8



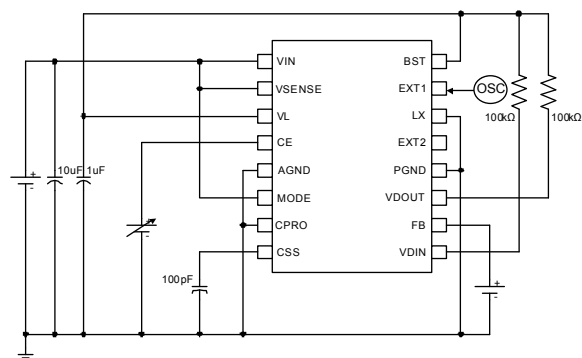
Circuit 9



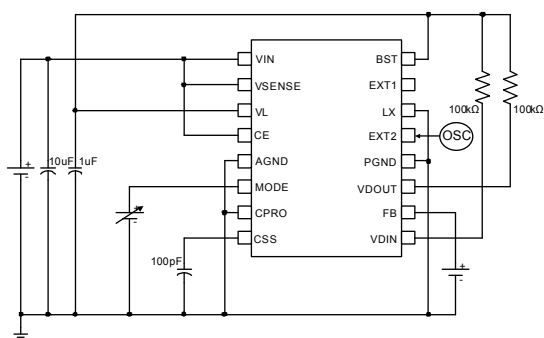
Circuit 10



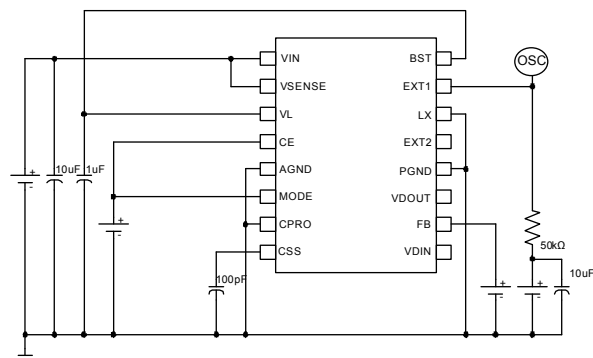
Circuit 11



Circuit 12

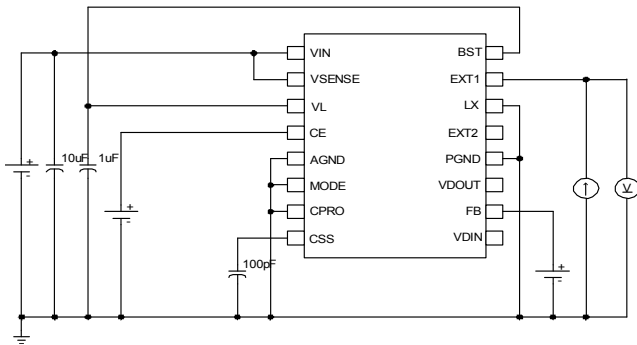


Circuit 13

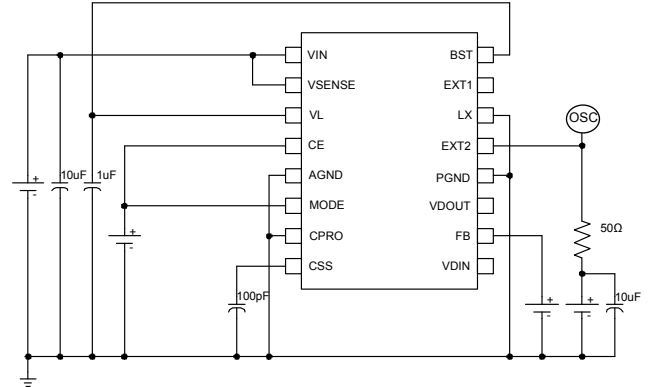


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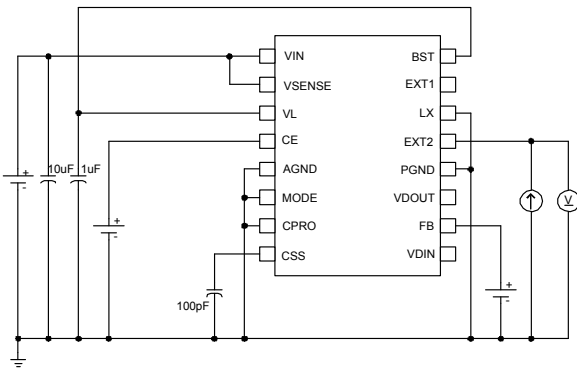
Circuit 14



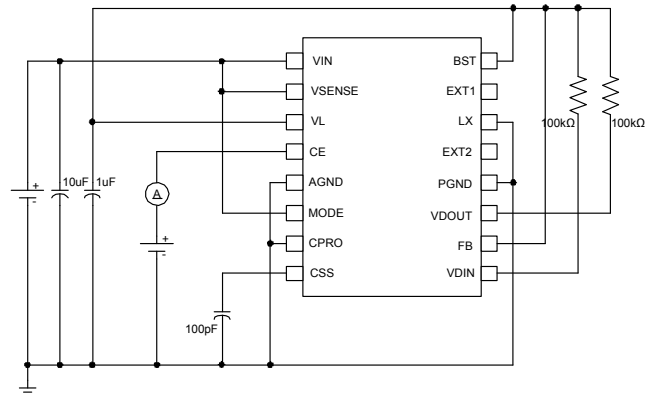
Circuit 15



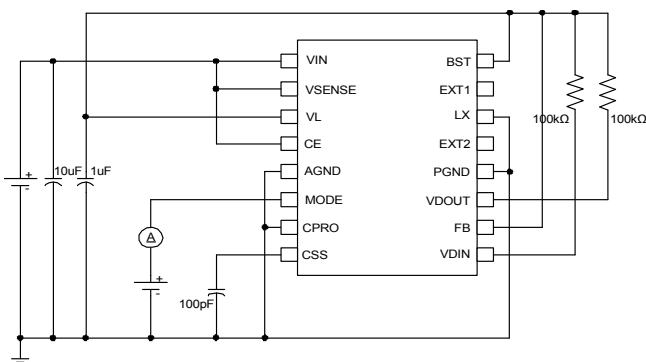
Circuit 16



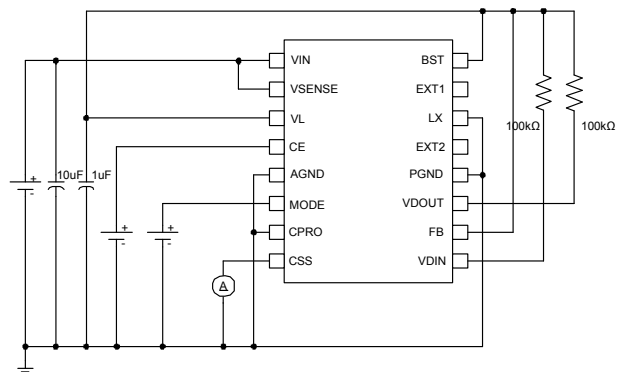
Circuit 17



Circuit 18



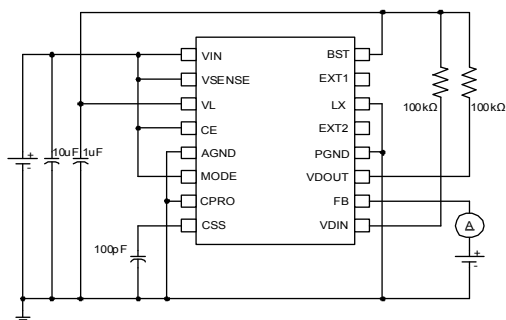
Circuit 19



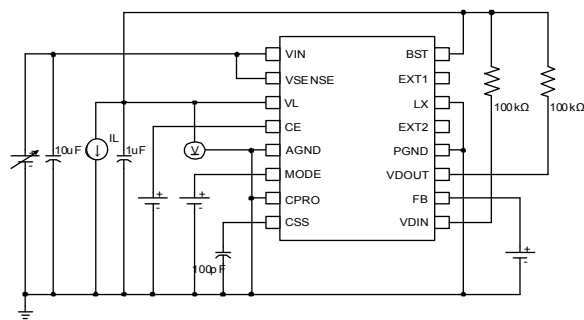


## ■ TEST CIRCUITS (Continued)

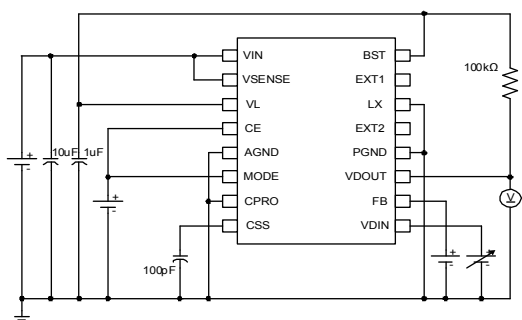
Circuit 20



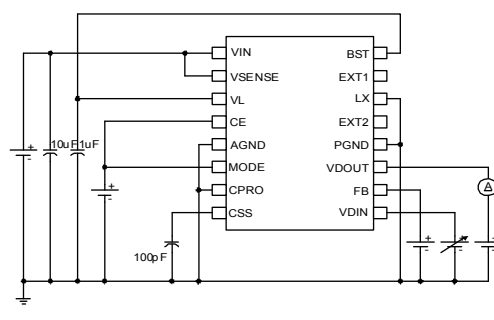
Circuit 21



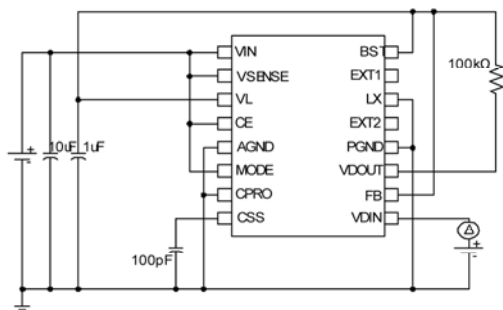
Circuit 22



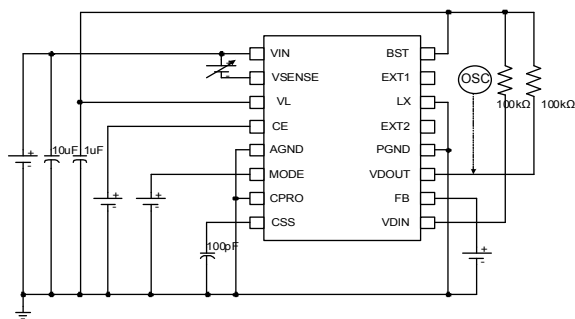
Circuit 23



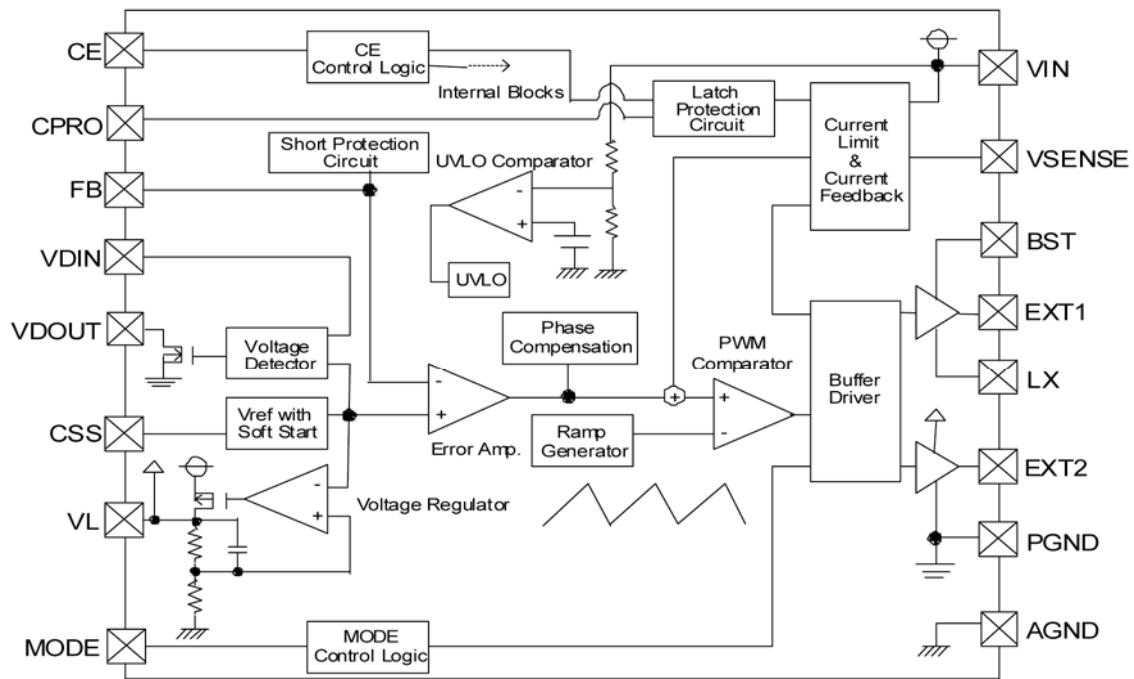
Circuit 24



Circuit 25



## ■ BLOCK DIAGRAM



## ■ OPERATIONAL EXPLANATION

### < Error Amplifier >

The error amplifier is designed to monitor output voltage. The amplifier compares the reference voltage with the feedback voltage. When a voltage lower than the reference voltage is fed back, the output voltage of the error amplifier increases.

### < Ramp Wave Generator >

The Ramp Wave Generator is organized by the circuits generates a saw-tooth waveform based on the oscillator circuit which sets an oscillation frequency and a signal from the oscillator circuit.

### < PWM Comparator >

The PWM Comparator compares outputs from the error amp. and saw-tooth waveform. When the voltage from the error amp's output voltage is low, the external switch will be set to OFF.

### < U.V.L.O. Comparator >

When the VIN pin voltage is lower than 1.5V (TYP.), the circuit sets EXT/2 to "L" and the external transistor is forced OFF.

### < Voltage Regulator >

The voltage regulator block generates 4.0V voltage for the bootstrap circuit. The regulator block is also the power supply for the internal circuit. Please do not use the regulator block as a local power supply.

### < Vref with Soft Start >

The reference voltage, Vref (FB pin voltage)=0.9V, is adjusted and fixed by laser trimming. The soft-start circuit protects against inrush current, when the power is switched on, and also to protect against voltage overshoot. It should be noted, however, that this circuit does not protect the load capacitor (CL) from inrush current. With the Vref voltage limited and depending upon the input to the error amps, the operation maintains a balance between the two inputs of the error amps and controls the EXT1 pin's ON time so that it doesn't increase more than is necessary.

### < CE Control Logic >

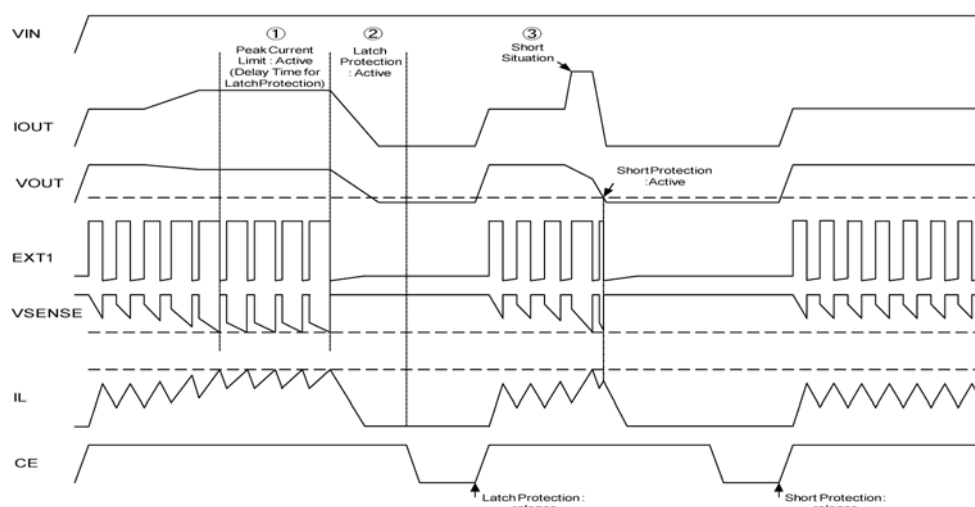
This function controls the operation and shutdown of the IC. When the voltage of the CE pin is 0.4V or less, the mode will be chip disable, the channel's operations will stop. The EXT1/2 pins will be kept at a low level (the external N-ch MOSFET will be OFF). When the CE pin is in a state of chip disable, current consumption will be no more than 4.0  $\mu$ A. When the CE pin's voltage is 1.4V or more, the mode will be chip enable and operations will recommence. With soft-start, 95% of the set output voltage will be reached within 8ms (CSS: 4700pF (TYP.)) from the moment of chip enable.

### < Voltage Detector >

The voltage detector of the XC9213 series is FB type. The reference voltage is 0.9V (TYP.) and the detect voltage can be set by external resistors. The output is N-ch Open Drain type. The detector is switched on / off with DC/DC by the CE pin.

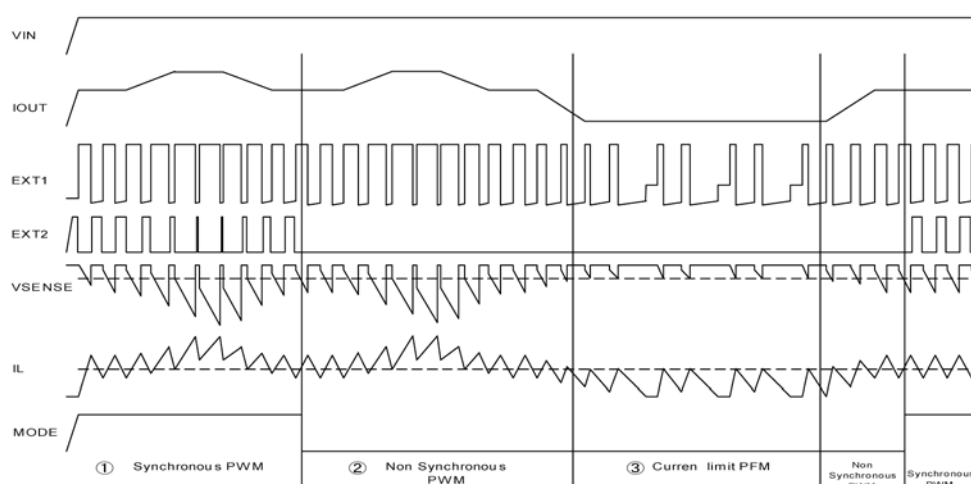
## ■ OPERATIONAL EXPLANATION (Continued)

### < Protection Circuit Operation (Current Limit, Latch Protection Circuit, and Short Protection Circuit) >



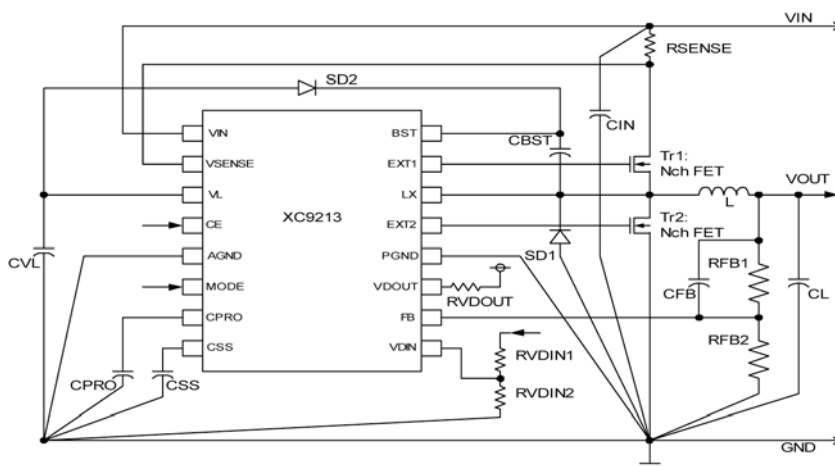
Shown above is a timing chart for protection circuit operations. When the output current changes from normal to an overcurrent condition, the current-limiting circuit detects the overcurrent condition as a voltage drop occurring, by virtue of the current-sensing resistor, at the VSENSE pin. Upon detection, the current-limiting circuit limits the peak current passed through the high-side N-ch MOSFET at every clock pulse (state ①). It is possible to regulate the value of limited current by varying the resistance value of the current-sensing resistor. A protection circuit (protective latch circuit), which is designed to stop the clock, functions if the overcurrent condition continues for a predetermined time (state ②). Time delay before the protective latch circuit functions is adjustable by the capacitance connected to the CPRO pin (typically 4.7 ms if CPRO has 4,700 pF). The protective latch circuit is reset by turning off and on, or by a disable action followed by an enable action using the CE pin. If, furthermore, the output is short-circuited (state ③) and VOUT decreases to a value close to 0 V, the short-circuit protection circuit detects the condition by means of the FB pin and stops the clock with no time delay. The short-circuit protection circuit is reset by turning off and on or by a disable action followed by an enable action using the CE pin, as with the protective latch circuit.

### < Mode Control Logic >



A timing chart for automatic switching of current-limiting PFM/PWM is shown above. High-level of the MODE pin allows PWM operations to occur for synchronous rectification (state ①). When the MODE pin shifts to low-level, current-limiting PFM/PWM automatic switching occurs with synchronous rectification stopped. Consequently, the low-side N-ch MOSFET is constantly off under this condition. In addition, a comparison is made for the purposes of automatic switching, between the ON time of the high-side N-ch MOSFET determined by the internal error amp. and the time required for the current passed at every clock pulse through the high-side N-ch MOSFET to reach a preset amount of current. The longer one is selected and becomes on duty (state ② or ③). If the time determined by the error amp. is longer than the other, PWM operation occurs. Current-limiting PFM operation occurs if the time taken by the current passing at every clock pulse to reach a preset amount of current is longer. Thus the automatic switching mechanism achieves high efficiency under light to heavy load conditions.

## ■ TYPICAL APPLICATION CIRCUIT



\*Please place C<sub>IN</sub> close to R<sub>SENSE</sub> as much as possible, so that an impedance does not occur between the elements.

\*Please place CIN, RSENSE, Tr1, Tr2, L, CL, and SD1 as close as possible to each other.

## ■ EXTERNAL COMPONENTS

\* Please refer to the DC/DC simulation section of the Torex web site (<http://www.torex.co.jp>) for more details.

- Recommended N-ch MOSFETs for Tr1 and Tr2

- IOUT: Less than 3A

PART NUMBER	MANUFACTURER	TYPE	Ciss (pF)	Crss (pF)	Crss / (Ciss + Crss)
uPA2751GR	NEC	Dual	1040	130	0.111
IRF7313	International Rectifier	Dual	650	130	0.167

- IOUT: More than 3A

PART NUMBER	MANUFACTURER	TYPE	Ciss (pF)	Crss (pF)	Crss / (Ciss + Crss)
SUD30N03	Vishay	Single	1170	30	0.049
SUD70N03	Vishay	Single	2700	360	0.118

\* It is recommended to use MOSFETs with Ciss less than 3000pF.

\* For Tr2, MOSFETs with smaller  $C_{rss} / (C_{iss} + C_{rss})$  are recommended.

- Recommended Coil (L)

PART NUMBER	MANUFACTURER
CDRH127/LD-7R4	SUMIDA
CDRH127-6R1	SUMIDA

\* For stable operation, please use a coil with L less than  $22 \mu\text{H}$ .

- Recommended Capacitor (C<sub>IN</sub>, C<sub>VL</sub>, C<sub>BST</sub>, C<sub>L</sub>)

COMPONENTS	PART NUMBER	MANUFACTURER	TYPE	VALUE	PCS
C <sub>IN</sub> (*1)	-	-	Ceramic	10 $\mu$ F	2
	25SC22M	SANYO	OS	22 $\mu$ F	1
CVL	-	-	Ceramic	1 $\mu$ F	1
CBST	-	-	Ceramic	1 $\mu$ F ~ 4.7 $\mu$ F	1
C <sub>L</sub> (*2)	20SS150M	SANYO	OS	150 $\mu$ F	1
	25PS100JM12	NIPPON CHEMI-CON	-	100 $\mu$ F	

(\*1)Please place C<sub>IN</sub> close to R<sub>SENSE</sub> as much as possible, so that an impedance does not occur between the elements.

A 1 $\mu$ F ceramic capacitor is recommended for CVL.

(\*2)Operation may become unstable if a ceramic capacitor is used for CL.

## EXTERNAL COMPONENTS (Continued)

### ●Output Voltage Setting ( $R_{FB1}$ , $R_{FB2}$ , $C_{FB}$ )

Output voltage can be set by adding external split resistors. Output voltage is determined by the following equation, based on the values of  $R_{FB1}$  and  $R_{FB2}$ . The sum of  $R_{FB1}$  and  $R_{FB2}$  should normally be  $2\text{ M}\Omega$  or less ( $R_{FB1} + R_{FB2} \leq 2\text{ M}\Omega$ ).

$$V_{OUT} = R_{FB1} / R_{FB2} + 1$$

The value of  $C_{FB}$ , speed-up capacitor for phase compensation, should be adjusted by the following equation.

$$f_{zfb} = 1 / (2 \times \pi \times C_{FB} \times R_{FB1}) \div 10\text{kHz}$$

Adjustments are required from 1kHz to 50kHz depending on the application, value of inductance (L), and value of load capacity (CL).

$V_{OUT}$ (V)	$R_{FB1}$ ( $\Omega$ )	$R_{FB2}$ ( $\Omega$ )	$C_{FB}$ (pF)
1.5	150	300	100
1.8	160	200	100
2.5	360	240	47
3.0	220	110	47
3.3	620	270	27
5.0	300	75	47

### ●Recommended Schottky Diode ( $SD1$ , $SD2$ )

SYMBOL	PART NUMBER	MANUFACTURER
SD1	CMS02	TOSHIBA
	DE5PC3	SHINDENGEN
SD2	XBS104S14R-G	TOREX
	CRS02	TOSHIBA

\*  $SD1$  and  $SD2$  should be of favorable reverse-current characteristics. If, in particular,  $SD2$  has poor reverse-current characteristics, CBST cannot be fully charged at high temperatures, resulting, in some cases, in failure to drive  $Tr1$ .

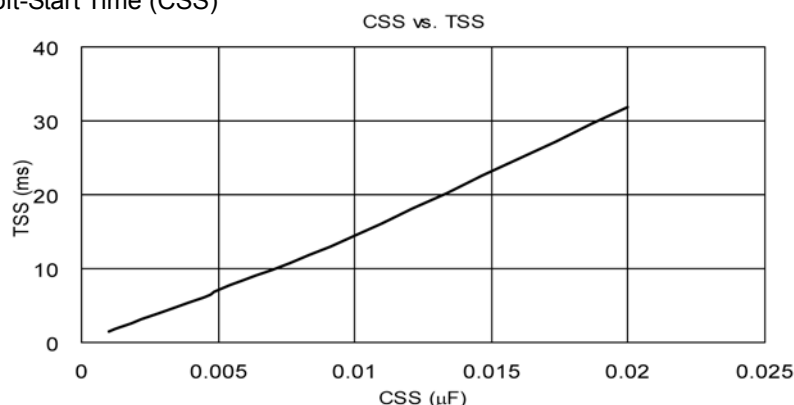
### ●Setting Latch Protection Circuit Delay Time (CPRO)

Time delay is 4.7 ms (TYP.) under the current conditions if CPRO has 4,700 pF. This time delay is roughly proportional to the value of CPRO.

ex.) When CPRO is 2200pF,  $4.7\text{ms (TYP.)} \times 2200\text{pF} / 4700\text{pF} = 2.2\text{ms (TYP.)}$   
 When CPRO is 0.01  $\mu\text{F}$  (10,000pF),  $4.7\text{ms (TYP.)} \times 10000\text{pF} / 4700\text{pF} = 10\text{ms (TYP.)}$

\* For stable operation, please use a capacitor with more than 2200pF as CPRO.

### ●Setting Soft-Start Time (CSS)



Relationships between the value of  $C_{ss}$  and the soft-start time (25°C TYP.) are shown at left. For stable operation, please use a capacitor with more than 2200pF as  $C_{ss}$ .

## EXTERNAL COMPONENTS (Continued)

### ● Sense Resistance (RSENSE)

The below values can be adjusted by using sense resistance (RSENSE).

It is recommended using the RSENSE value in the range of 20mΩ to 100mΩ.

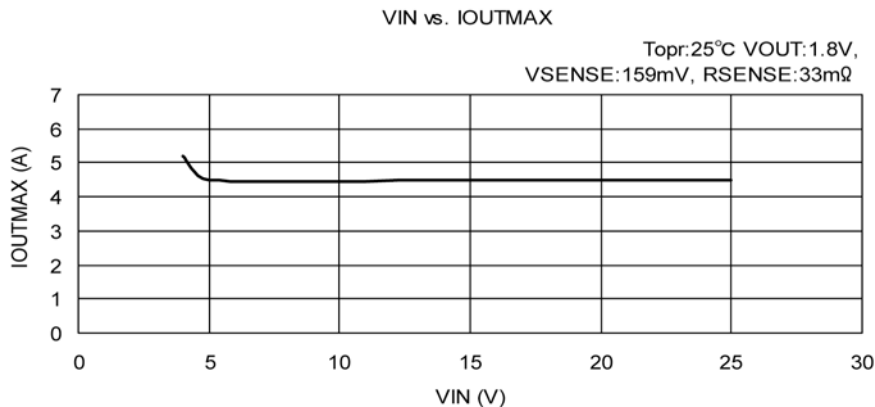
#### 1) Detect current value of the overcurrent detect circuit

Maximum output current (IOUTMAX) can be adjusted as the equation below.

$$I_{OUTMAX} (A) \div 200mV (MAX.) / R_{SENSE} (m\Omega)$$

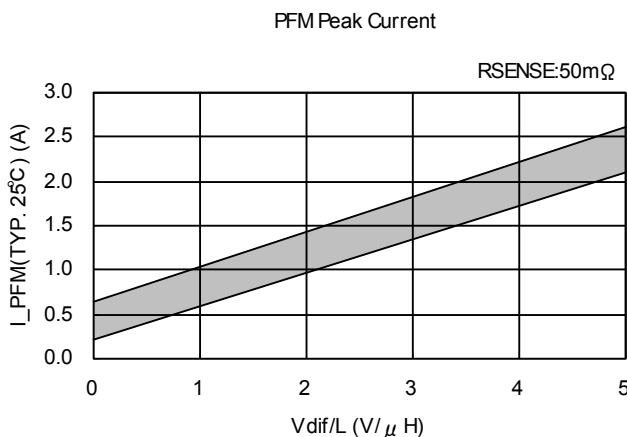
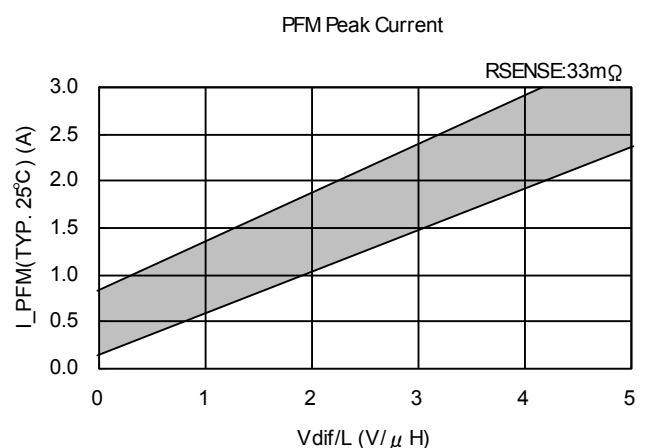
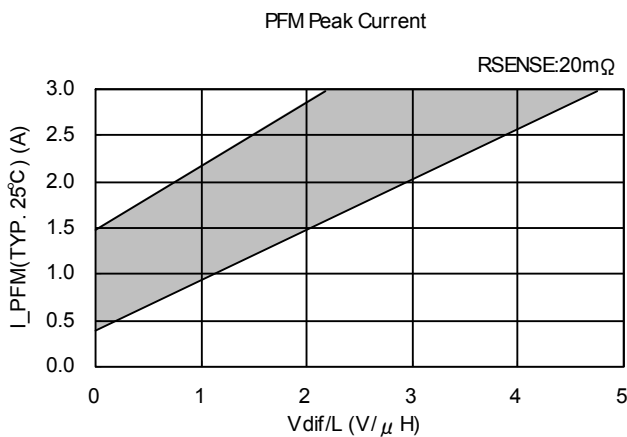
When  $4V \leq V_{IN} < 5V$ , the maximum output current becomes larger than the calculated value.

Please also refer to the characteristics performance below.



#### 2) Peak current value of the current limit PFM control

Peak current value of the current limit PFM control (I\_PFM) varies depending on the dropout voltage (VDIF), the coil (L) value and the sense resistance value (RSENSE). For the XC9213 series' sample with voltage sense (VSENSE) 170mV, the characteristic performance below shows the changes in the peak current (I\_PFM) when the sense resistance values (RSENSE) are 20mΩ, 33 mΩ, and 50 mΩ. The peak current varies according to the dropout voltage and the coil value.



The sense voltage varies within the range of  $145\text{ mV} \leq V_{SENSE} \leq 200\text{ mV}$ .  
The peak current as shown in three graphs fluctuates according to the sample's sense voltage.

## ■ EXTERNAL COMPONENTS (Continued)

### ● Divided Resistors For VD Input Voltages (R<sub>VDIN1</sub>, R<sub>VDIN2</sub>)

Detect voltage of the detector block can be adjusted by the external divided resistors for VD input voltages (RVDIN1, RVDIN2) as the equation below.

When  $0.855V \leq V_{DF} \leq 0.925V$  (0.9V TYP.)

$$\text{Detect voltage} = V_{DF} \times (R_{VDIN1} + R_{VDIN2}) / R_{VDIN2} \text{ [V]}$$

Please select RVDIN1 and RVDIN2 as the sum of RVDIN1 and RVDIN2 becomes less than  $2M\Omega$ .

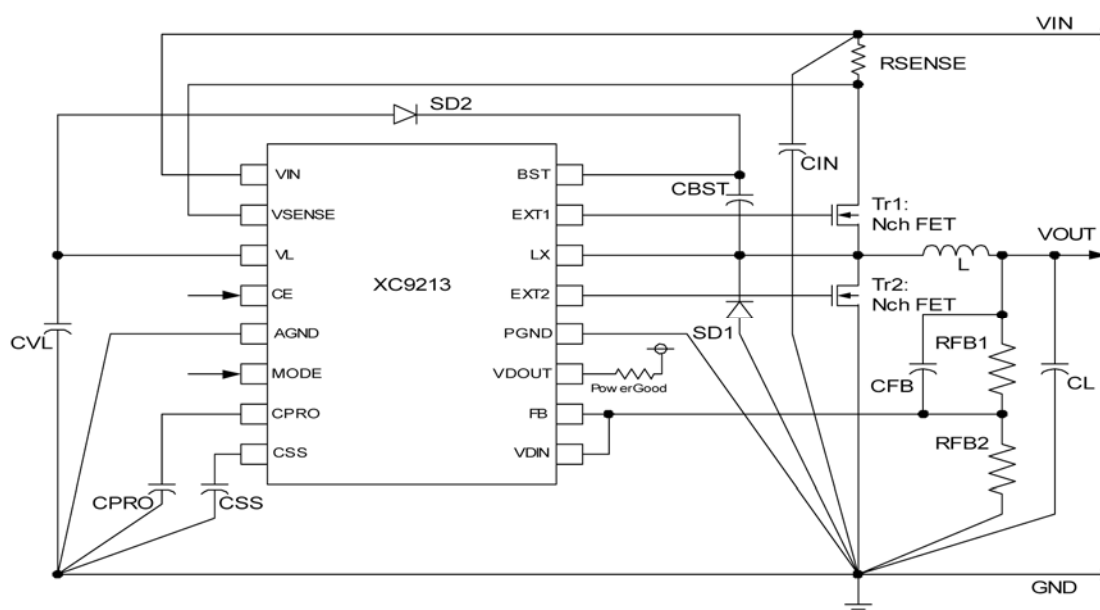
●Divided Resistor For VD Output Voltage (R<sub>VDOUT</sub>)

Output type of the detector block is N-channel open drain. Please use a 1k $\Omega$  resistor or more as RVDOUT.

## ■ APPLICATION CIRCUIT EXAMPLE

The application circuit shown below is the example for using the detector block as power good.

Please connect the VDIN pin with the FB pin as below.



## NOTES ON USE

### 1. Overcurrent Limit Function

The internal current detection circuit is designed to monitor voltage occurs between R<sub>SENSE</sub> resistors in the overcurrent condition. In case that the overcurrent limit function operates when the output is shorted, etc., the current detection circuit detects that the voltage between R<sub>SENSE</sub> resistors reaches the SENSE voltage (170mV TYP.), and, thereby, the overcurrent limit circuit outputs the signal, which makes High side's N-ch MOSFET turn off. Therefore, delay time will occur (300ns TYP.) after the current detection circuit detects the SENSE voltage before High side's N-ch MOSFET turns off. When the overcurrent limit function operates because of rapid load fluctuation etc., the SENSE voltage will spread during the delay time without being limited at the voltage value, which is supposed to be limited. Therefore, please be noted to the absolute maximum ratings of external MOSFET, a coil, and an Schottky diode.

### 2. Short Protection Circuit

In case that a power supply is applied to the IC while the output is shorted, or the IC is switched to enable state from disable state via the CE pin, when High side's N-ch MOSFET is ON and Low side's N-ch MOSFET is OFF, the potential difference for input voltage will occur to the both ends of a coil. Therefore, the time rate of coil current becomes large. By contrast, when High side's N-ch MOSFET is OFF and Low side's N-ch MOSFET is ON, there is almost no potential difference at both ends of the coil since the output voltage is shorted to the Ground. For this, the time rate of coil current becomes quite small. This operation is repeated within soft-start time; therefore, coil current will increase for every clock. Also with the delay time of the circuit, coil current will be converged on a certain current value without being limited at the current amount, which is supposed to be limited. However, step-down operation will stop and the circuit can be latched if FB voltage is decreasing to the voltage level, which enables to operate a short protection circuit when the soft-start time completes. Even if the FB voltage is not decreasing to the voltage level, which a short protection circuit cannot be operated, the step-down operation stops when CPRO time completes, and the circuit will be latched.

Please be noted to the absolute maximum ratings of external MOSFET, a coil, and an Schottky diode.

### 3. Current Limit PFM Control

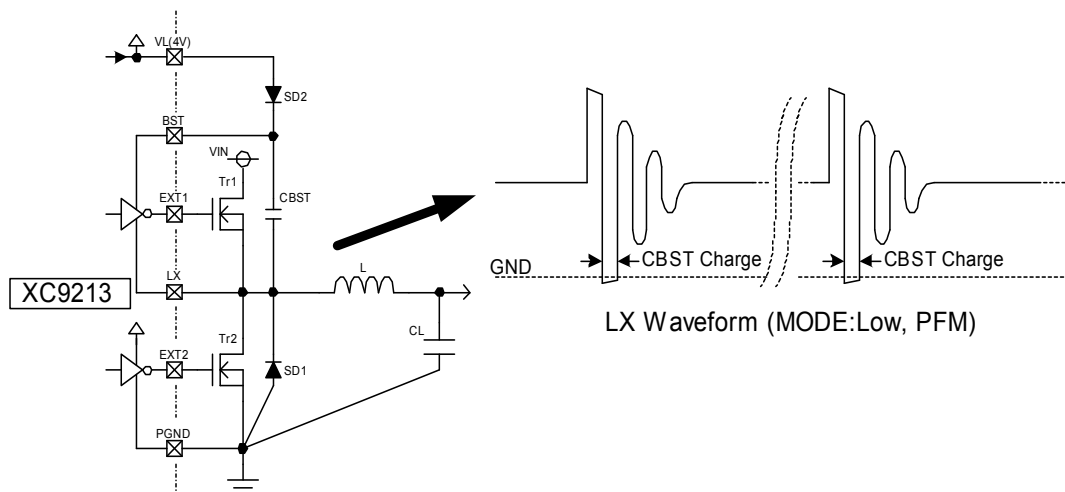
With a built-in bootstrap buffer driver circuit, the XC9213 series generates voltage for Tr1 to be turned on by charging CBST with VL (4V). When Tr1 is off, Tr2 is on, and the Lx signal is low, it will be suitable timing for charging CBST. (Please refer to the above figure.) For that reason, at PFM control (MODE: Low), the clock pulses will decrease extremely according to the decrease of the load current. As a result, it will cause a decrease of charging frequency and an electric discharge of CBST so that sufficient voltage for the Tr1 to be turned on will not be supplied.

Therefore,

1) Please use a Schottky Barrier Diode with few reverse current values for SD2.

2) Please avoid extreme light loads (e.g. less than a few mA)

Moreover, the above-mentioned operation may occur, influenced by external components including SD2 and ambient temperature. It's recommended to use the IC after evaluation with an actual device.





## ■ NOTES ON USE (Continued)

### 4. Switching on and off the IC by the input voltage pin

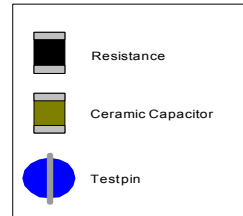
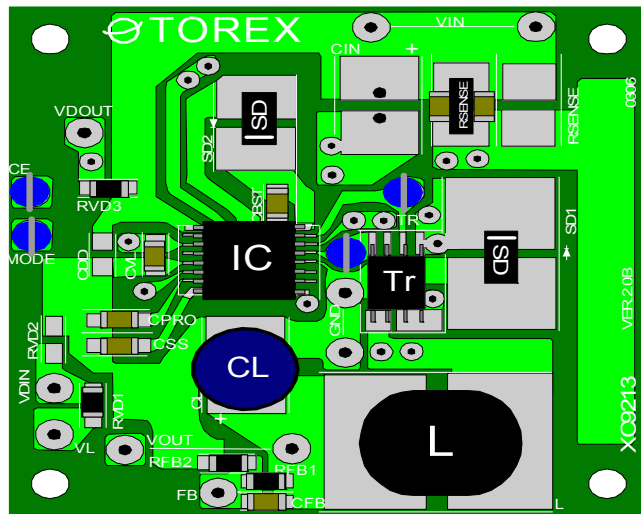
When the IC is switched on and off by the input voltage pin (VIN) instead of the chip enable pin (CE), the IC may stop operation because a protection circuit built inside the short-protection circuit, etc. begins to work in order to block ON signal which is sent before the soft-start capacitor connection pin (Css) resets. The following methods can be used for avoiding this situation;

- a) Turn on the power source again after input voltage becomes below U.V.L.O. detect voltage (1.0V MIN.), furthermore, after the lapse of the time constant of  $\tau = C_{ss} \times 50k$ .
- b) Before turning the power source on again, start-up the IC after resetting the Css forcibly and keeping soft-start time.

Please make sure the Css pin is discharged once and the soft-start time is secured when starting up the IC.

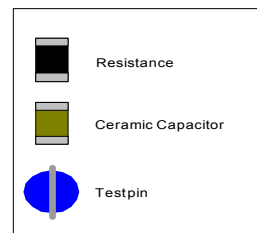
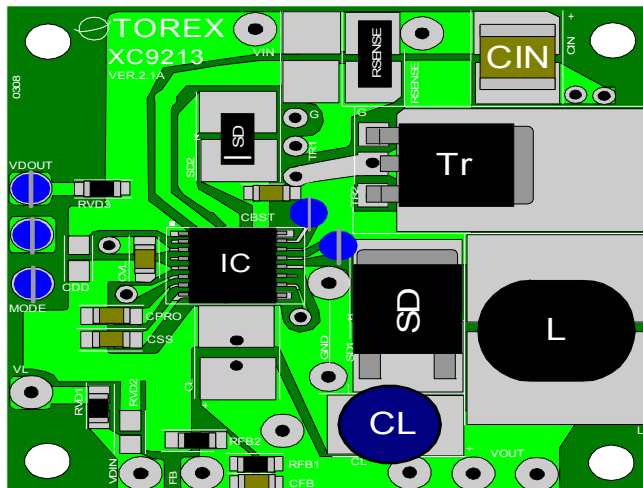
## REFERENCE PCB LAYOUT

### Layout For Using a Dual MOSFET

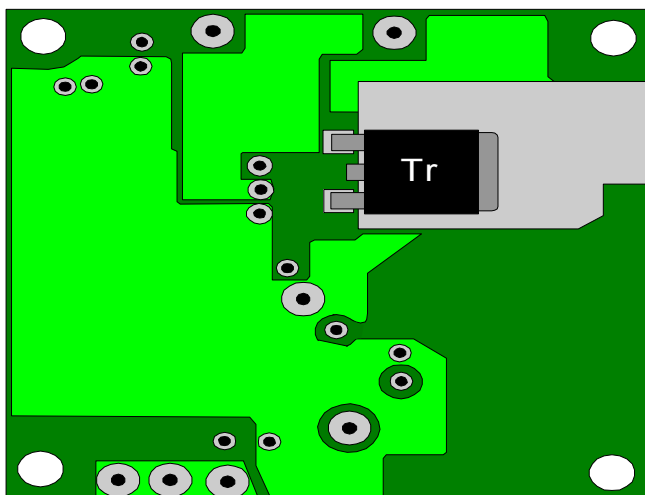


### Layout For Using a Single MOSFET

<TOP VIEW>



<BOTTOM VIEW>

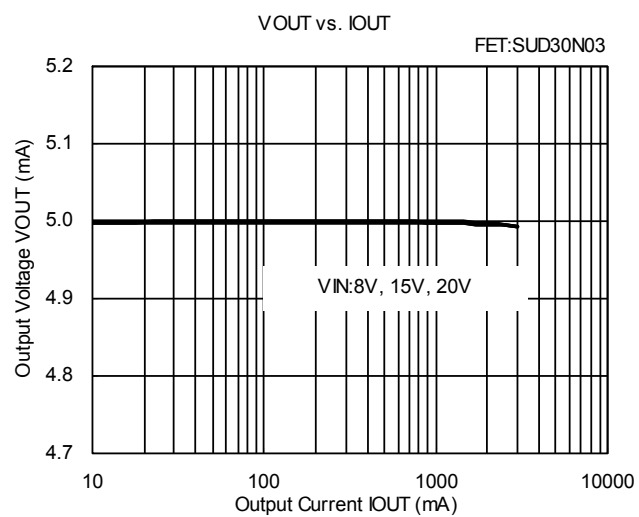
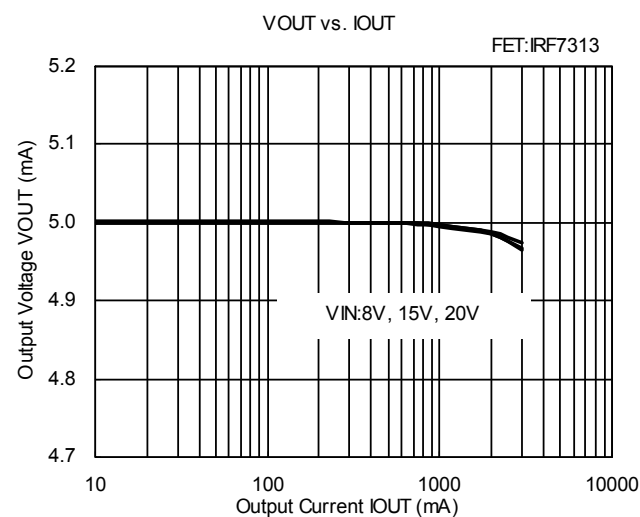
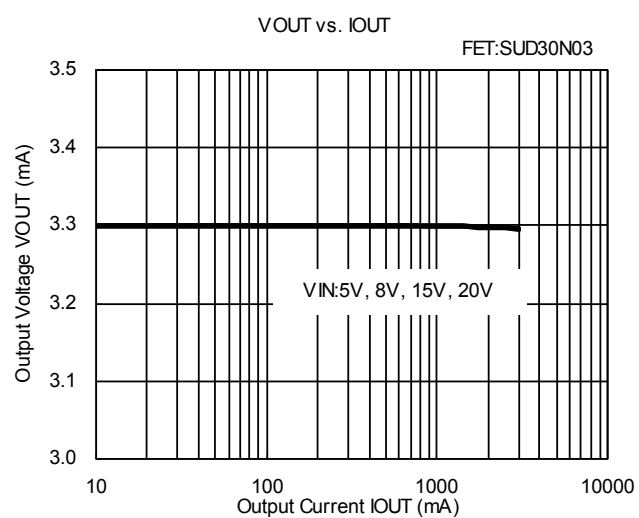
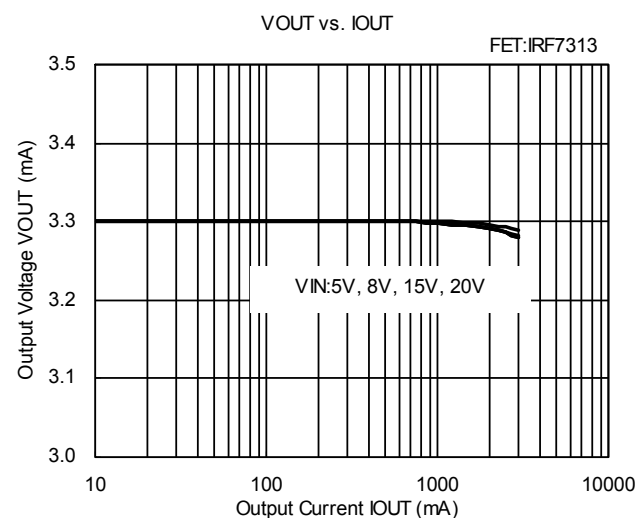
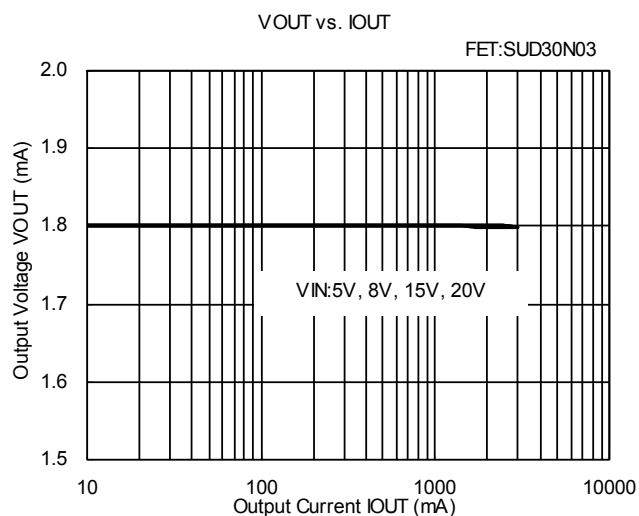
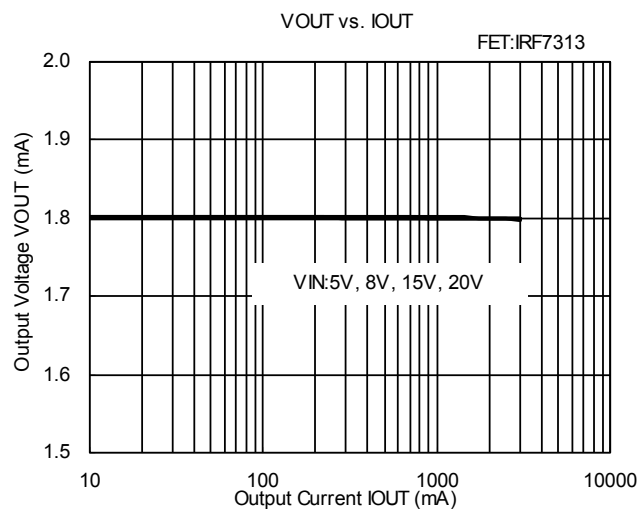


- \* Please use tinned wires etc. for the VIN, the VOUT, and the GND.
- \*\* Please attach test pins etc. to the CE, the MODE, the EXT, and the EXT2.
- \*\*\* Please solder mount the RSENSE and the CE as close as possible.

## TYPICAL PERFORMANCE CHARACTERISTICS

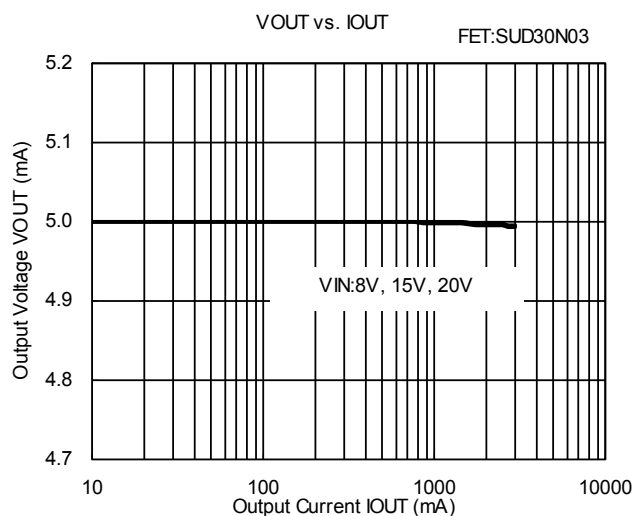
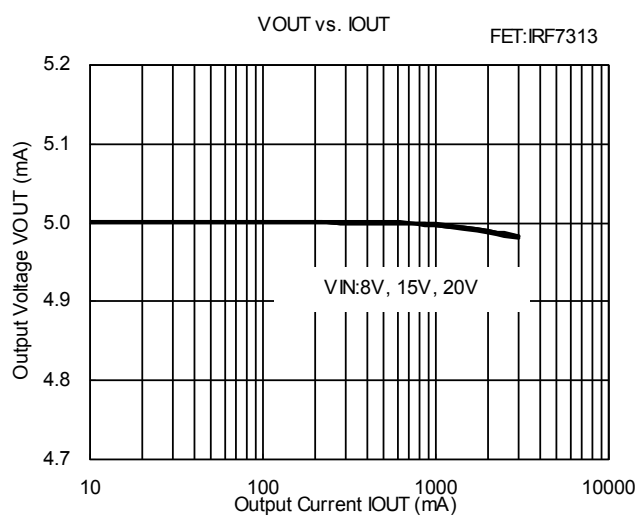
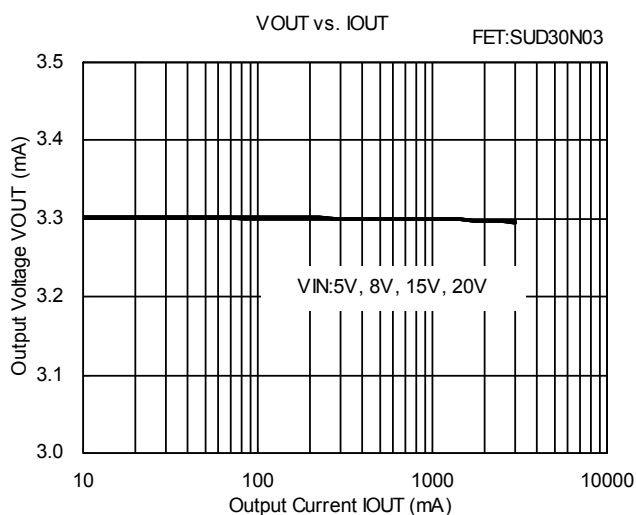
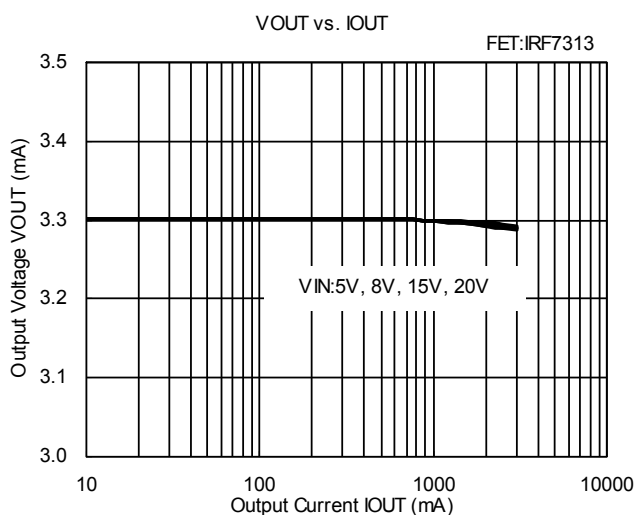
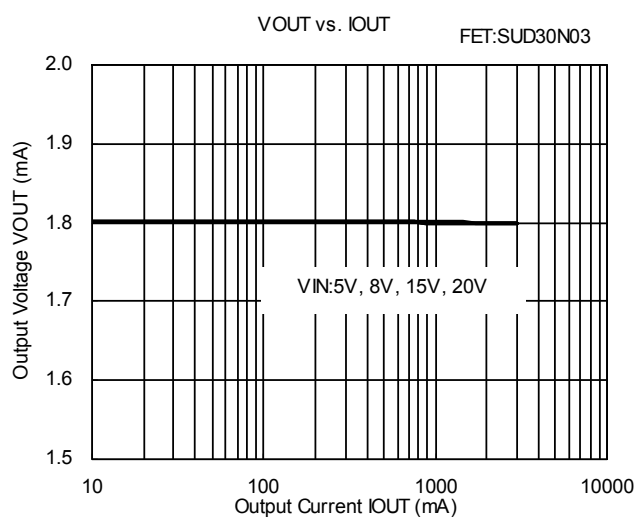
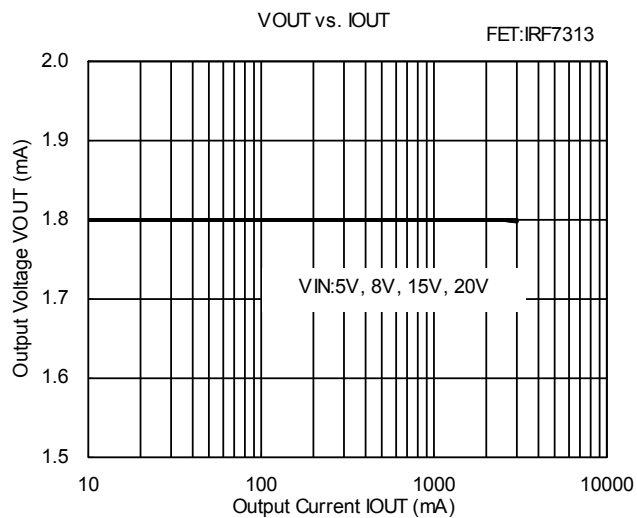
(Unless otherwise stated, Topr:25°C)

(1) Output Voltage vs. Output Current <MODE: High>



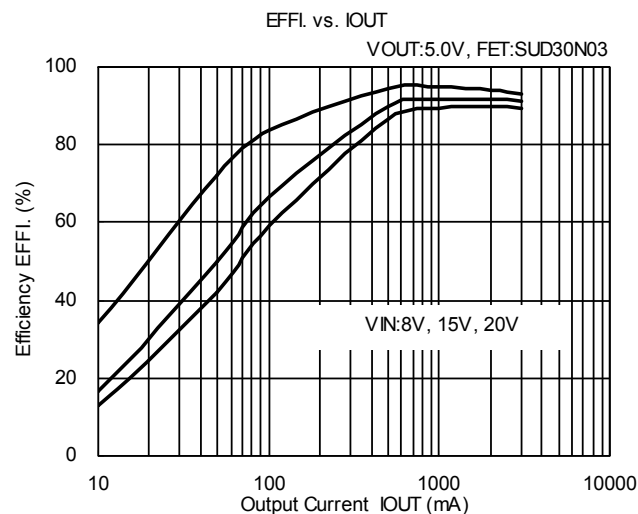
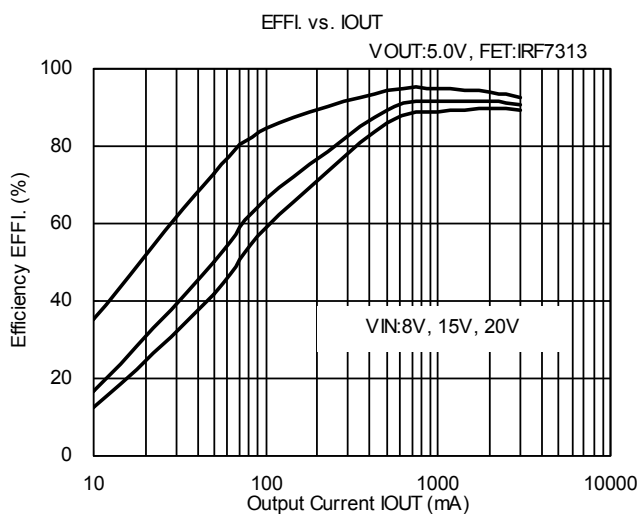
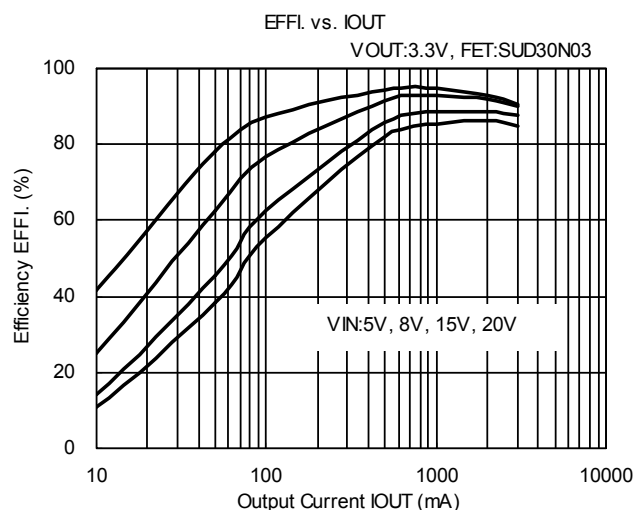
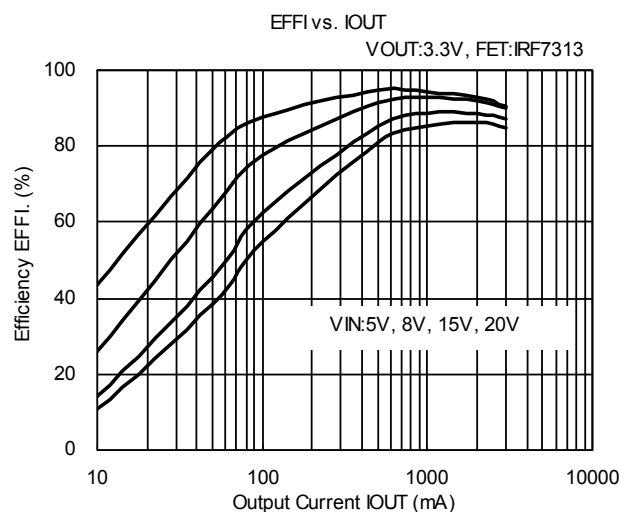
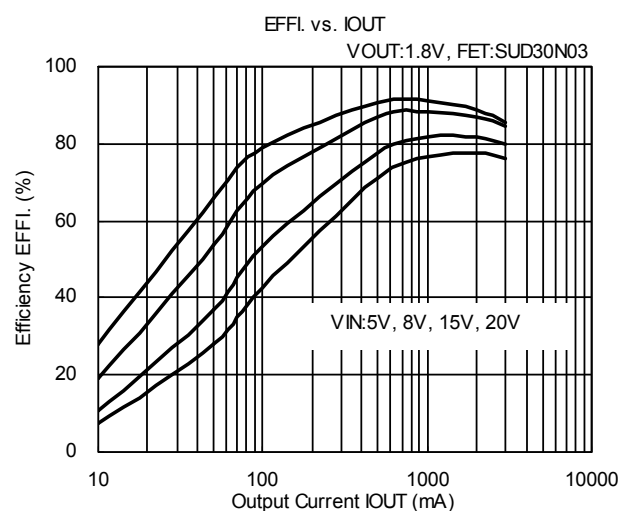
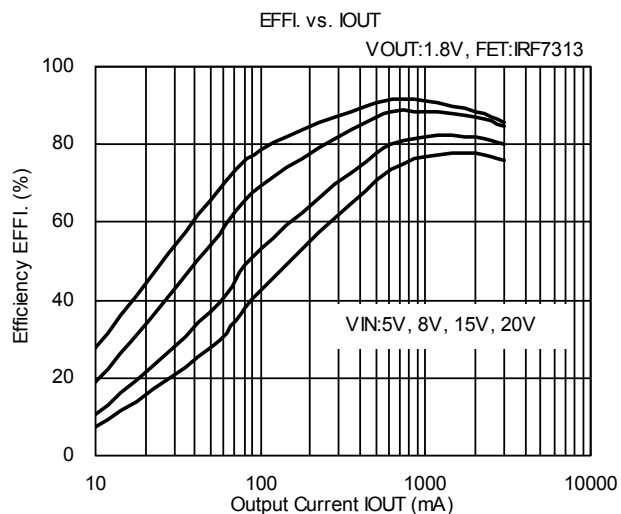
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(2) Output Voltage vs. Output Current <MODE: Low>



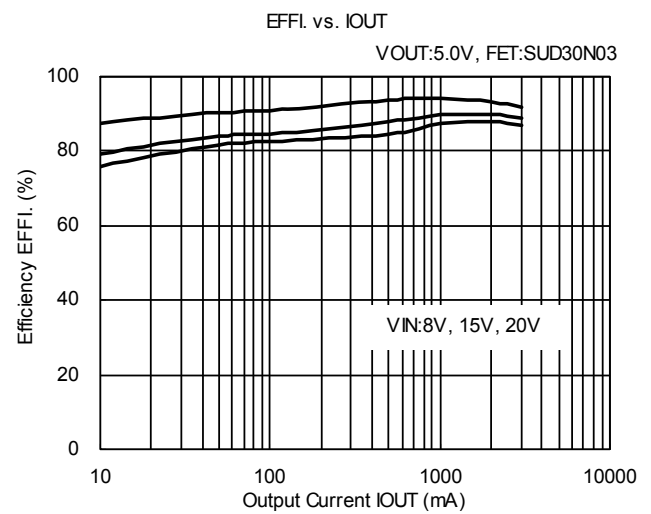
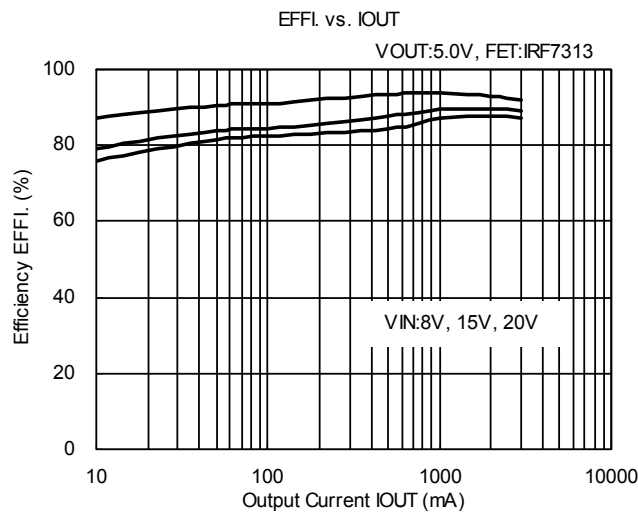
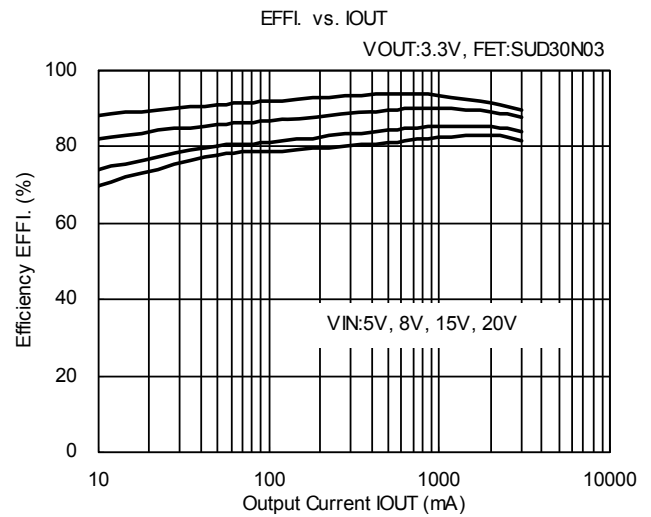
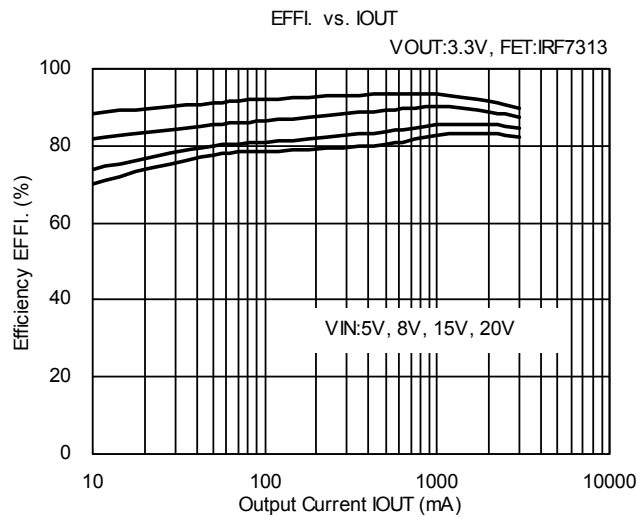
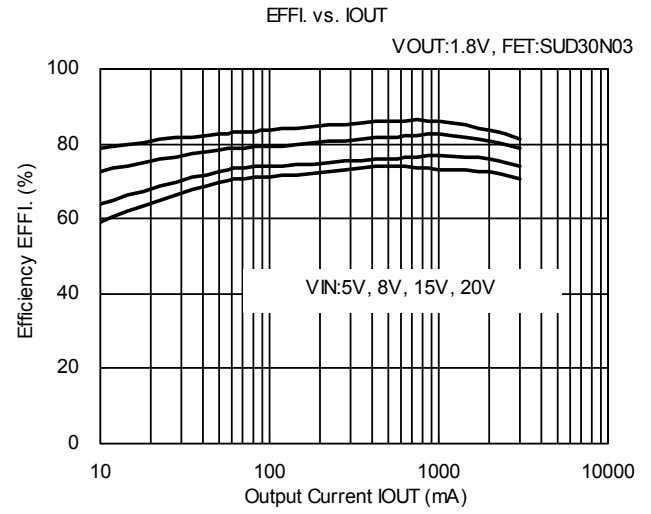
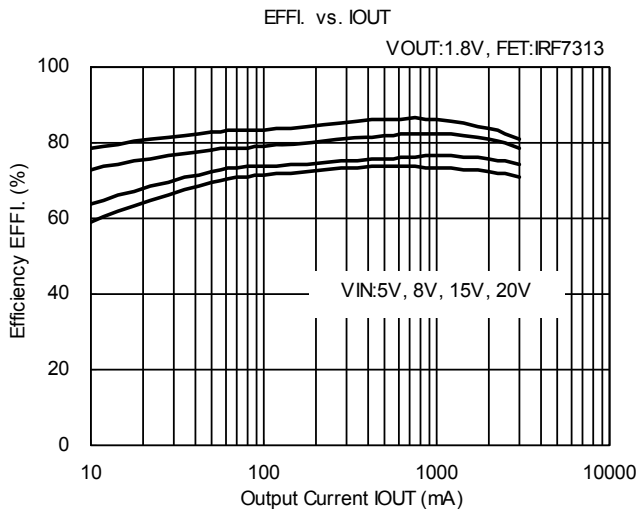
## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(3) Efficiency vs. Output Current <MODE: High>



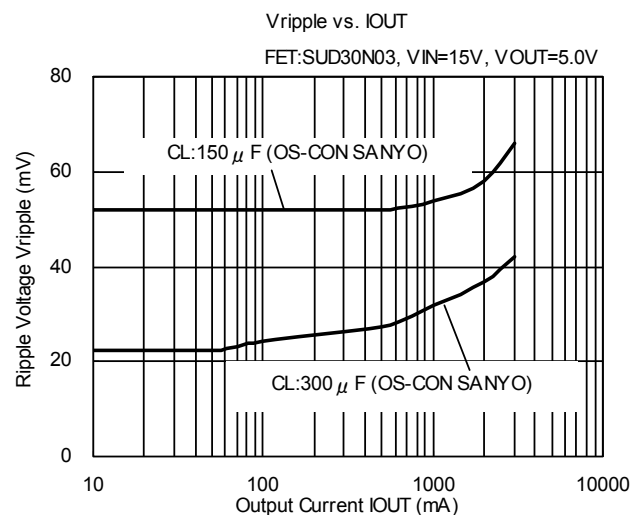
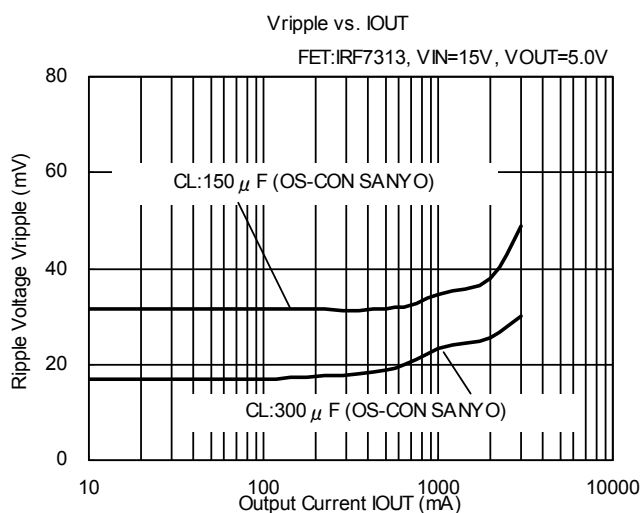
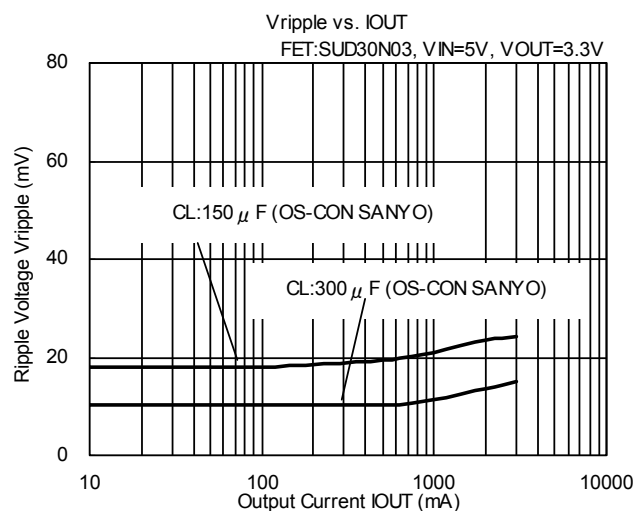
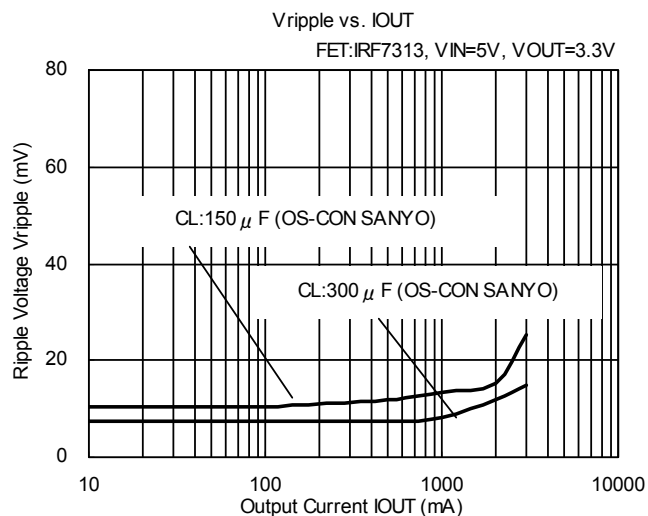
## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(4) Efficiency vs. Output Current <MODE: Low>

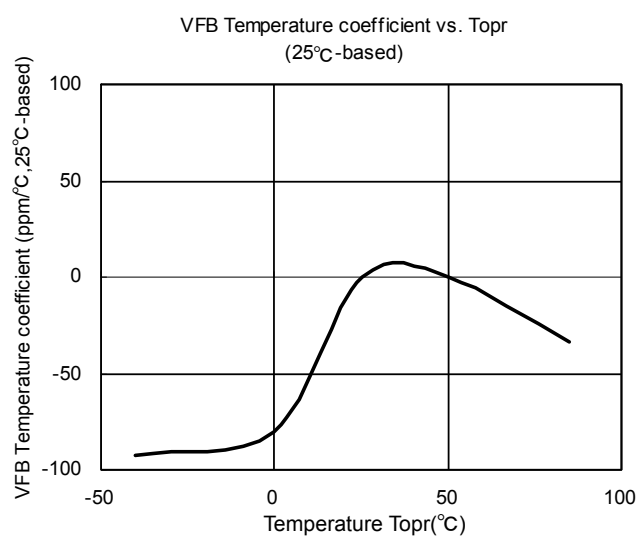
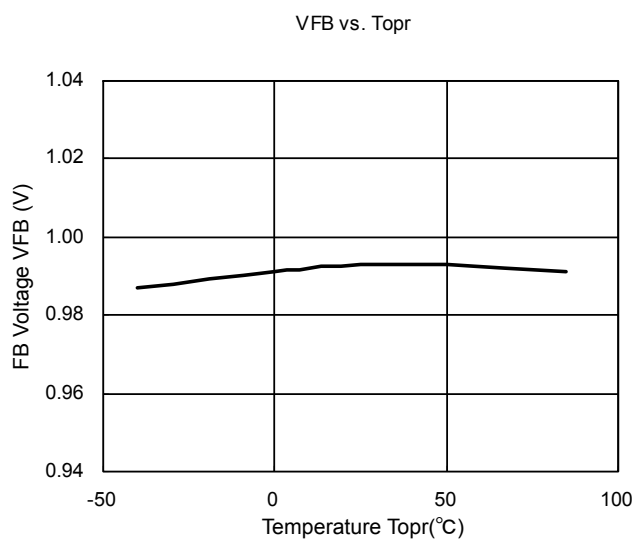


## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(5) Ripple Voltage vs. Output Current <MODE: High, Coil: CDRH127/LD-7R4>

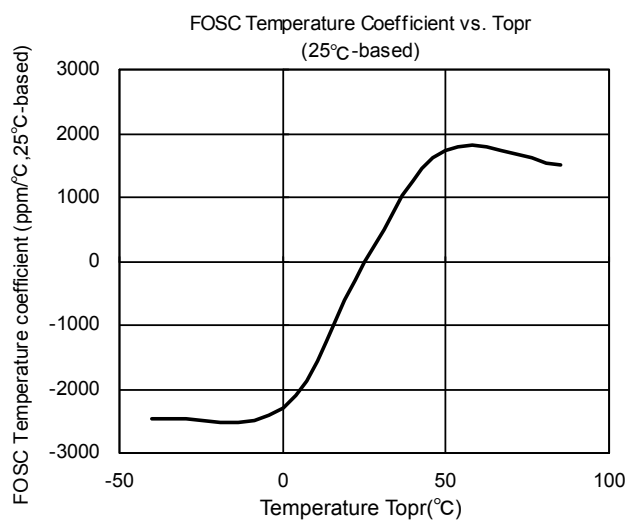
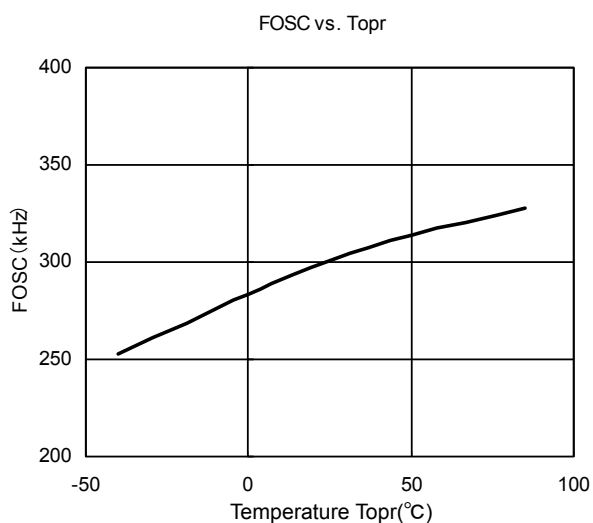


(6) FB Voltage Temperature Characteristics

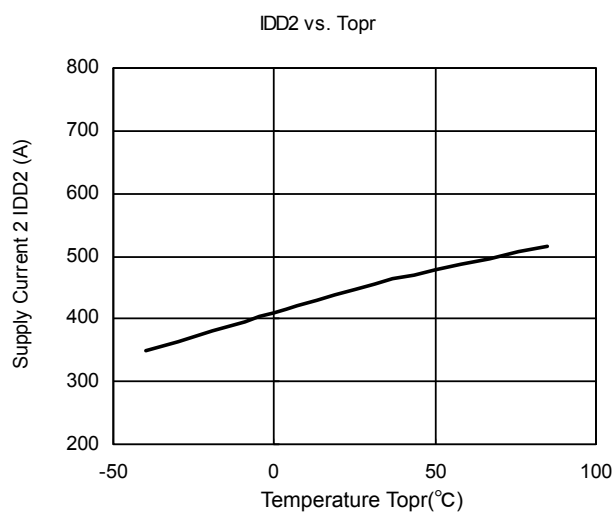
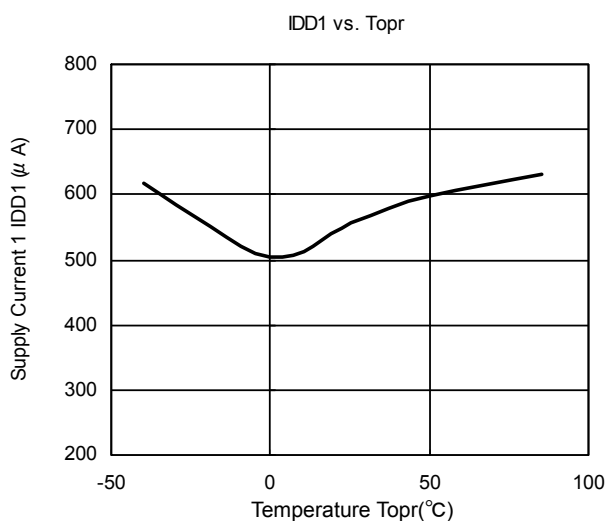


## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

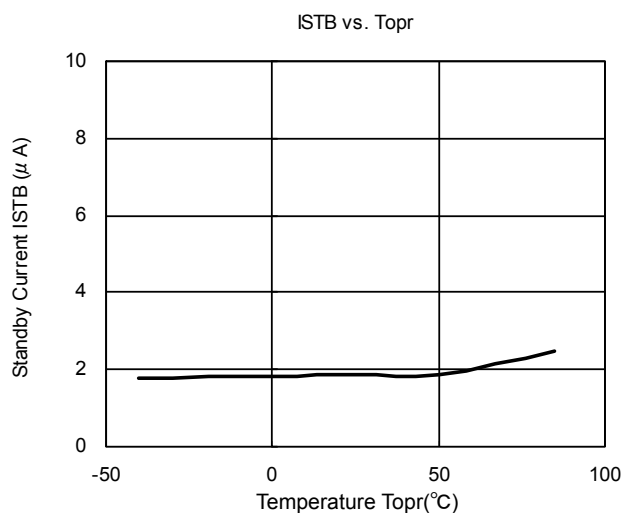
### (7) Oscillation Frequency Temperature Characteristics



### (8) Supply Current 1 & 2 Temperature Characteristics



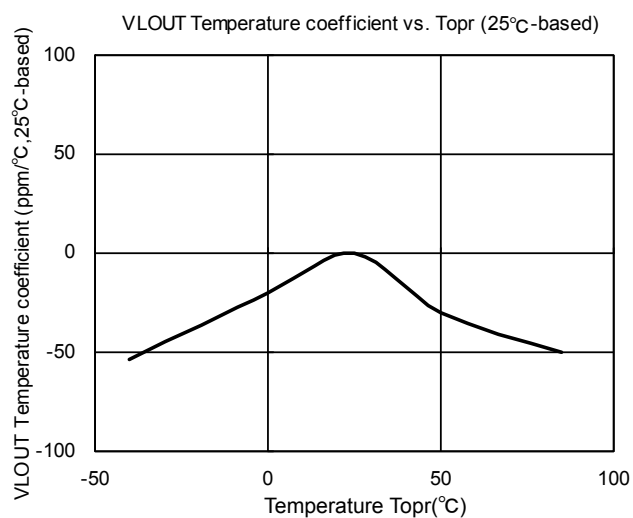
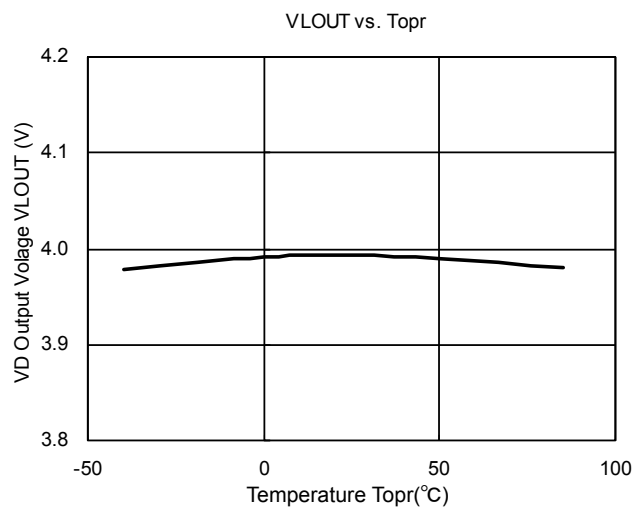
### (9) Stand-by Current Temperature Characteristics



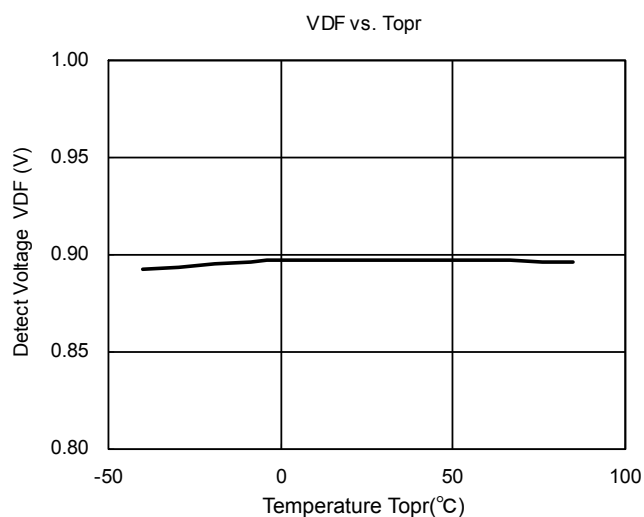


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

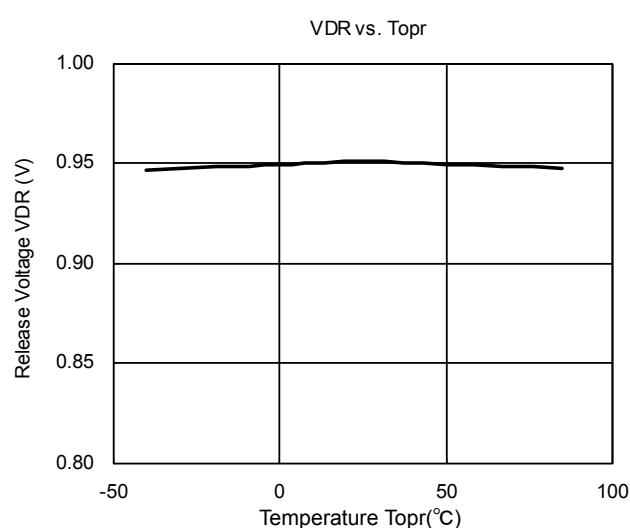
(10) VR Output Voltage Temperature Characteristics



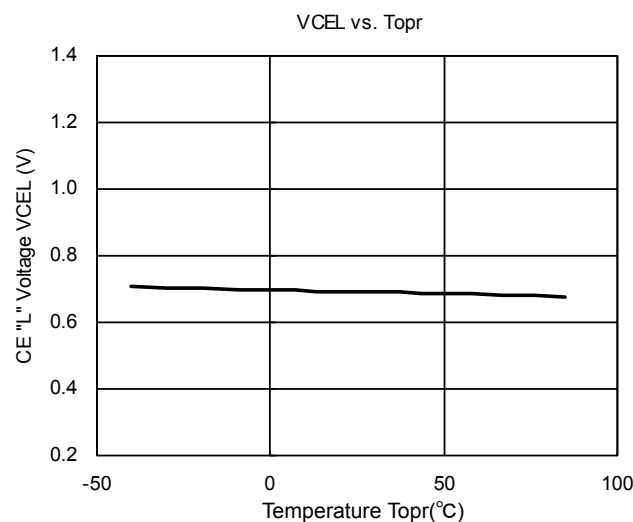
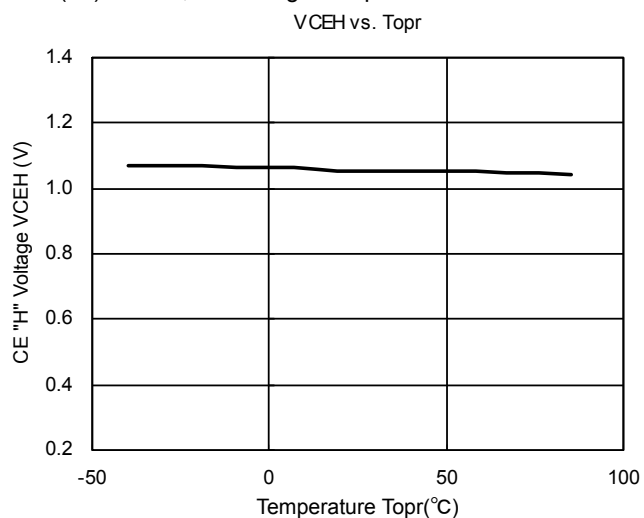
(11) VD Detect Voltage Temperature Characteristics



(12) VD Release Voltage Temperature Characteristics

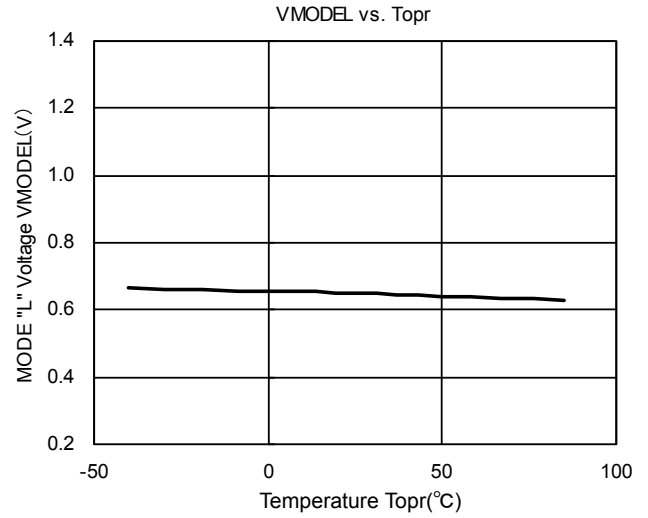
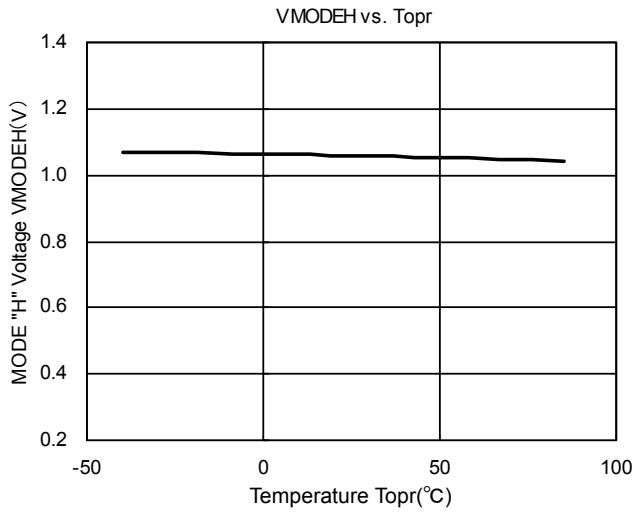


(13) CE "H", "L" Voltage Temperature Characteristics

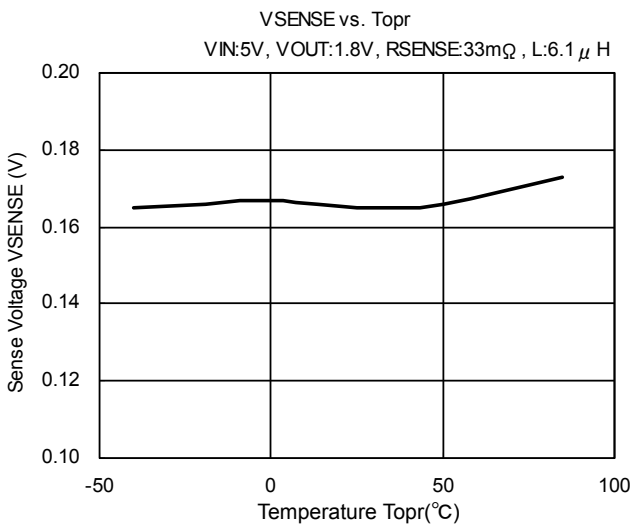


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

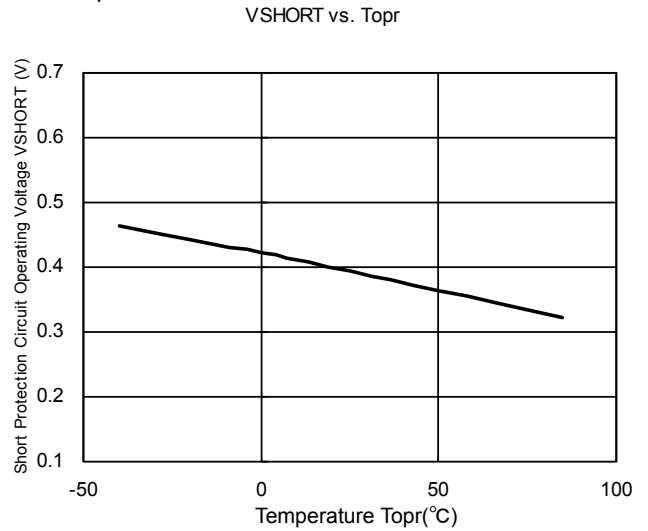
(14) MODE "H", "L" Voltage Temperature Characteristics



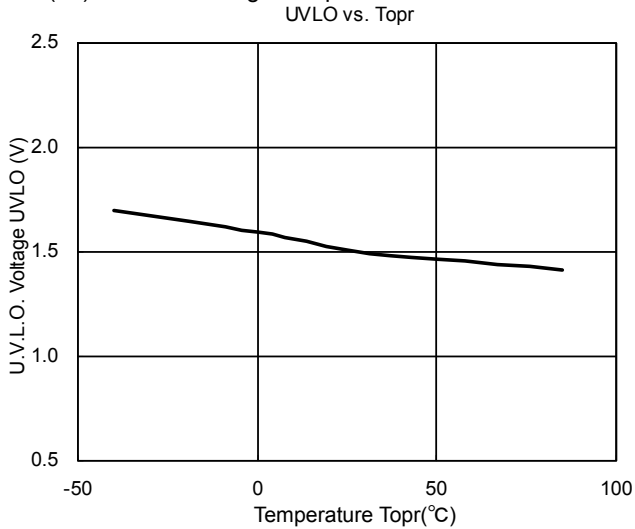
(15) Sense Voltage Temperature Characteristics



(16) Short Protection Circuit Operation Voltage Temperature Characteristics



(17) U.V.L.O. Voltage Temperature Characteristics



## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (18) Load Transient Response Characteristics <MODE: High>

<Condition>

V<sub>IN</sub>: 5V

V<sub>OUT</sub>: 1.8V

I<sub>OUT</sub>: 0A ↔ 1A

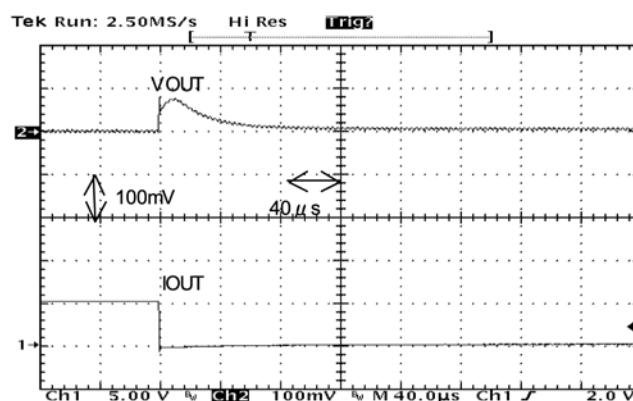
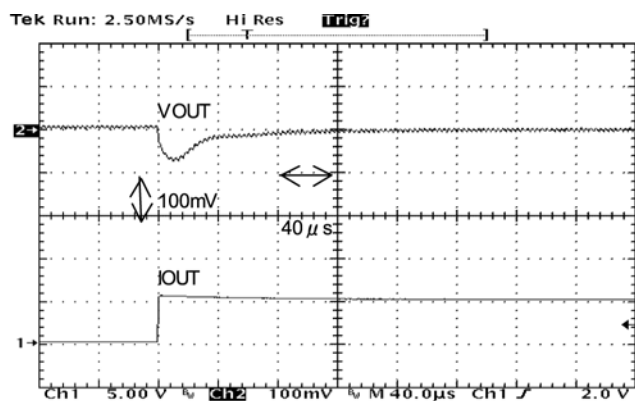
MODE: High

FET: IRF7313 (International Rectifier)

R<sub>SENSE</sub>: 33mΩ

CL: 150μF (OS-CON, SANYO)

L: CDRH127/LD-7R4 (SUMIDA)



<Condition>

V<sub>IN</sub>: 15V

V<sub>OUT</sub>: 1.8V

I<sub>OUT</sub>: 0A ↔ 1A

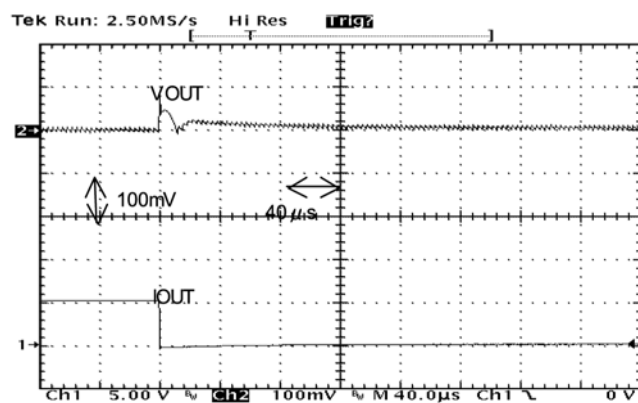
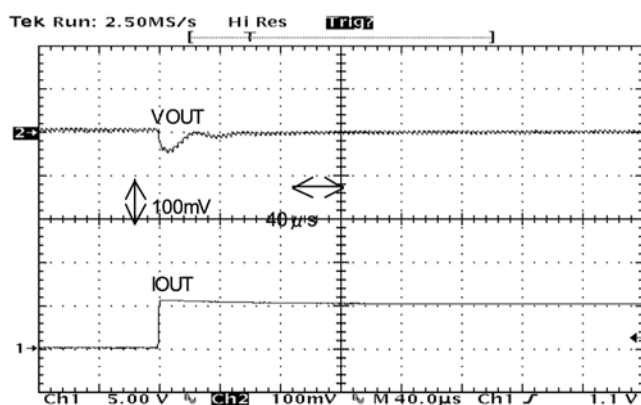
MODE: High

FET: IRF7313 (International Rectifier)

R<sub>SENSE</sub>: 33mΩ

CL: 150μF (OS-CON, SANYO)

L: CDRH127/LD-7R4 (SUMIDA)



<Condition>

V<sub>IN</sub>: 5V

V<sub>OUT</sub>: 3.3V

I<sub>OUT</sub>: 0A ↔ 1A

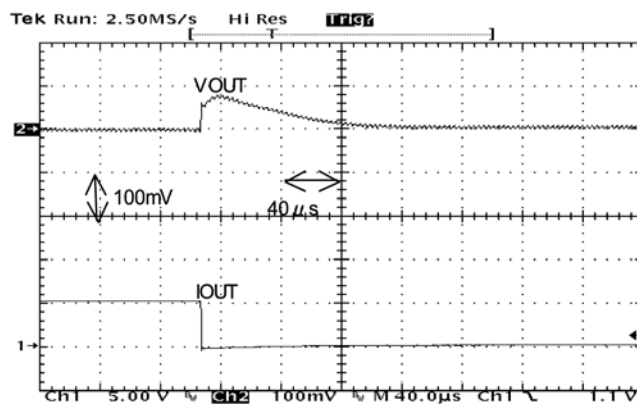
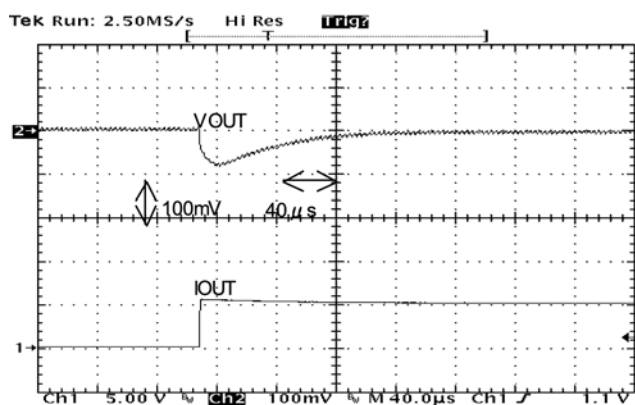
MODE: High

FET: IRF7313 (International Rectifier)

R<sub>SENSE</sub>: 33mΩ

CL: 150μF (OS-CON, SANYO)

L: CDRH127/LD-7R4 (SUMIDA)



## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (18) Load Transient Response Characteristics <MODE: High> (Continued)

<Condition>

VIN: 15V

VOUT: 3.3V

IOUT: 0A  $\leftrightarrow$  1A

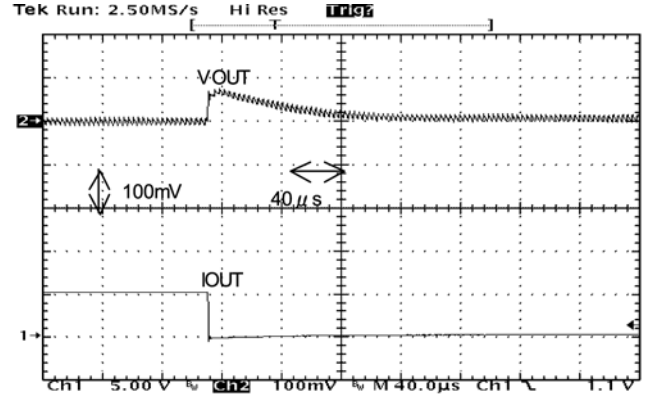
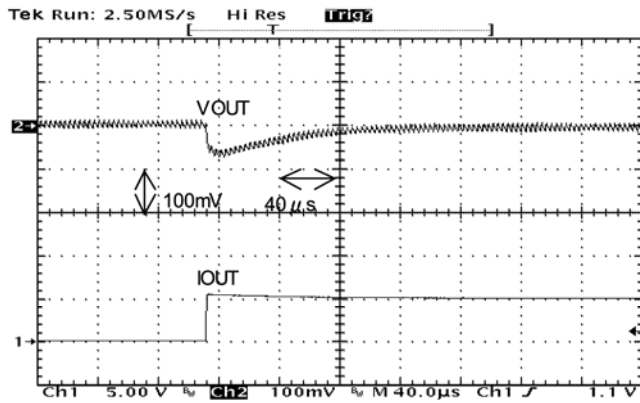
MODE: High

FET: IRF7313 (International Rectifier)

RSENSE: 33m $\Omega$

CL: 150 $\mu$ F (OS-CON, SANYO)

L: CDRH127/LD-7R4 (SUMIDA)



<Condition>

VIN: 5V

VOUT: 1.8V

IOUT: 0A  $\leftrightarrow$  1A

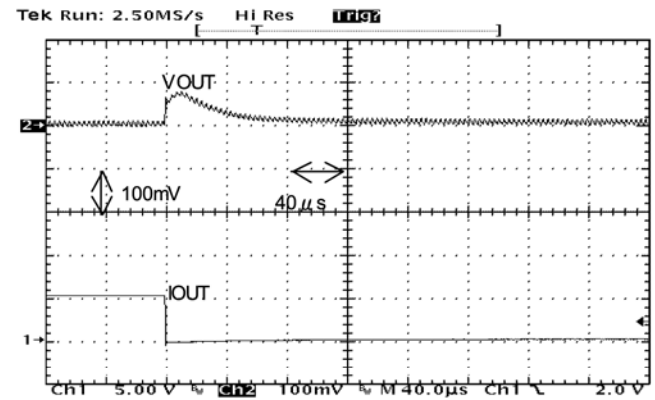
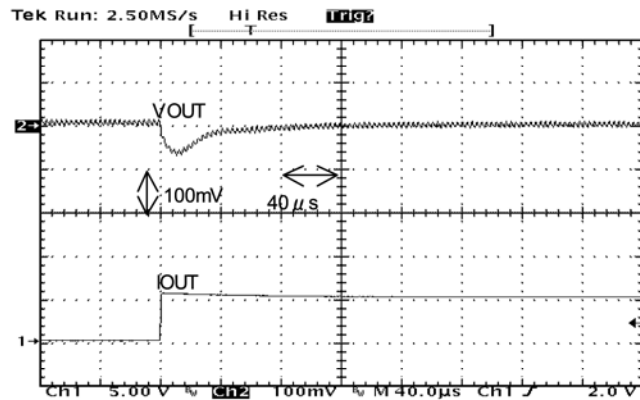
MODE: High

FET: SUD30N03 (Vishay)

RSENSE: 33m $\Omega$

CL: 150 $\mu$ F (OS-CON, SANYO)

L: CDRH127/LD-7R4 (SUMIDA)



<Condition>

VIN: 15V

VOUT: 1.8V

IOUT: 0A  $\leftrightarrow$  1A

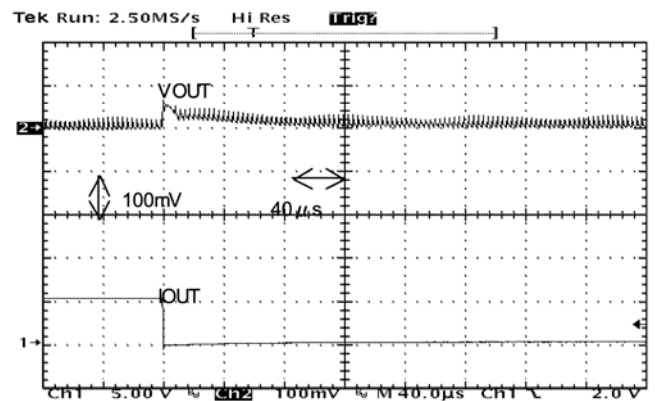
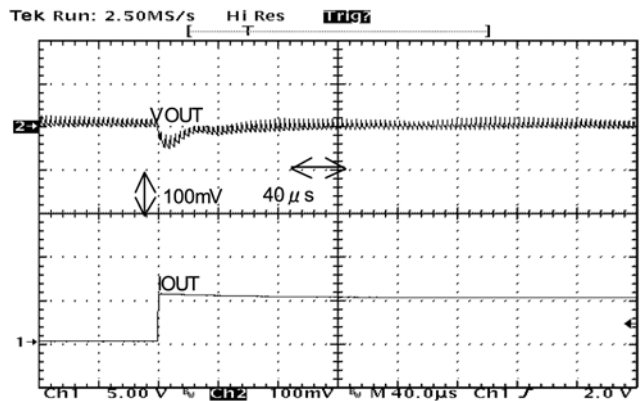
MODE: High

FET: SUD30N03 (Vishay)

RSENSE: 33m $\Omega$

CL: 150 $\mu$ F (OS-CON, SANYO)

L: CDRH127/LD-7R4 (SUMIDA)



## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(18) Load Transient Response Characteristics <MODE: High> (Continued)

<Condition>

VIN: 5V

VOUT: 3.3V

IOUT: 0A  $\leftrightarrow$  1A

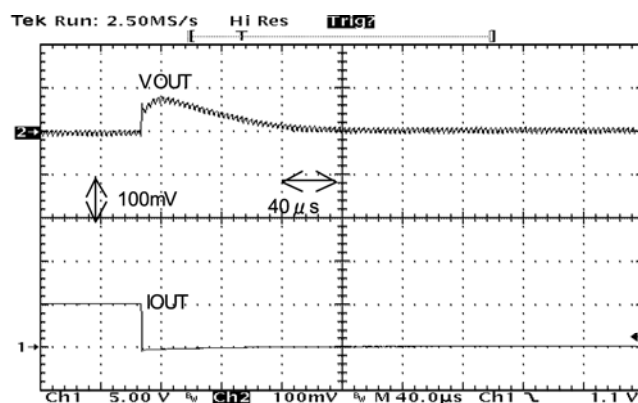
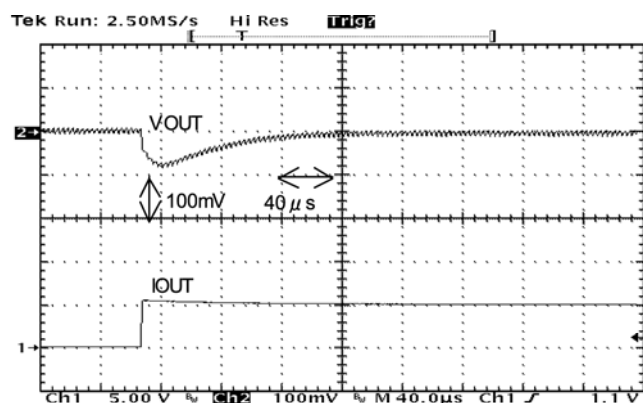
MODE: High

FET: SUD30N03 (Vishay)

RSENSE: 33m $\Omega$

CL: 150  $\mu$ F (OS-CON, SANYO)

L: CDRH127/LD-7R4 (SUMIDA)



<Condition>

VIN: 15V

VOUT: 3.3V

IOUT: 0A  $\leftrightarrow$  1A

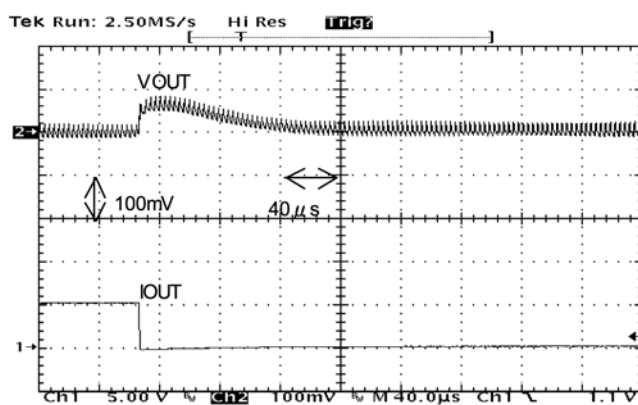
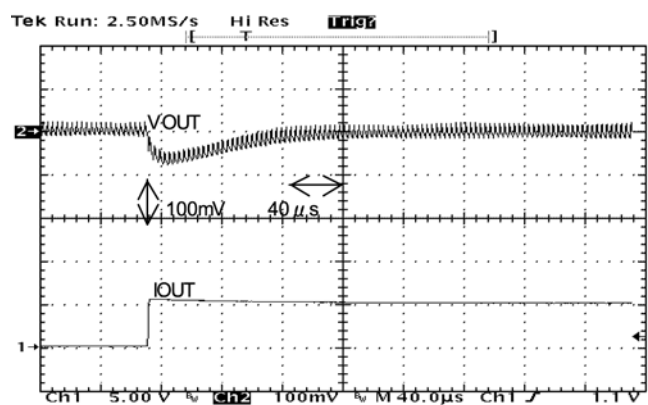
MODE: High

FET: SUD30N03 (Vishay)

RSENSE: 33m $\Omega$

CL: 150  $\mu$ F (OS-CON, SANYO)

L: CDRH127/LD-7R4 (SUMIDA)



## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (19) Load Transient Response Characteristics <MODE: Low>

<Condition>

V<sub>IN</sub>: 5V

V<sub>OUT</sub>: 1.8V

I<sub>OUT</sub>: 0A  $\leftrightarrow$  1A

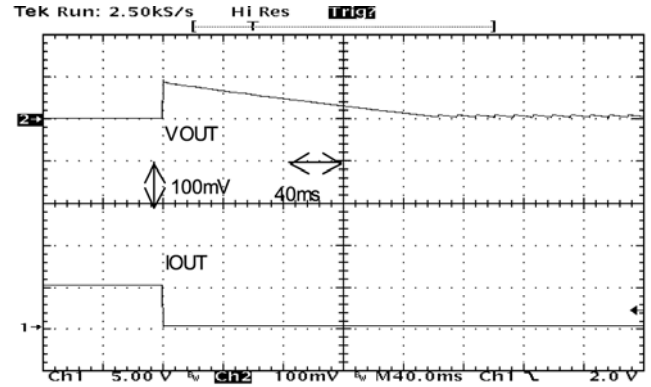
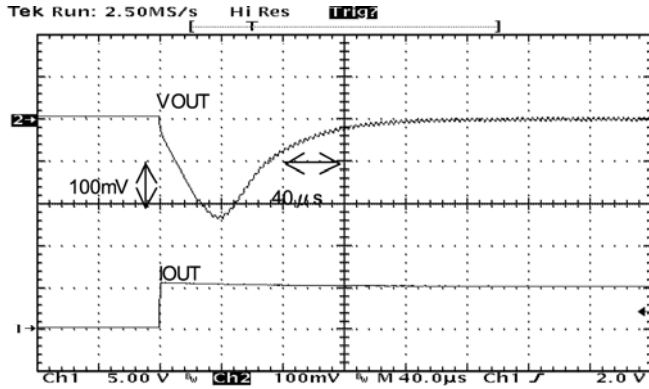
MODE: Low

FET: IRF7313 (International Rectifier)

R<sub>SENSE</sub>: 33m $\Omega$

C<sub>L</sub>: 150 $\mu$ F (OS-CON, SANYO)

L: CDRH127/LD-7R4 (SUMIDA)



<Condition>

V<sub>IN</sub>: 5V

V<sub>OUT</sub>: 1.8V

I<sub>OUT</sub>: 0A  $\leftrightarrow$  1A

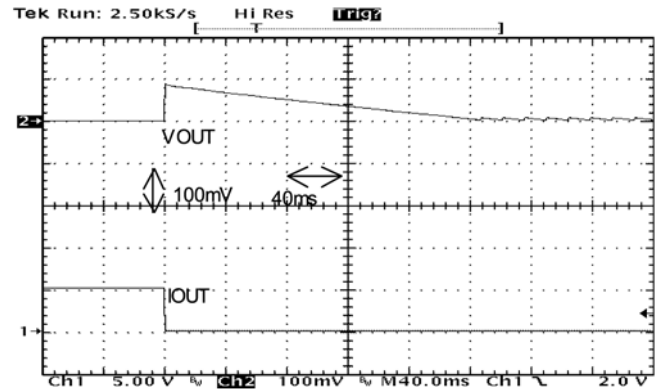
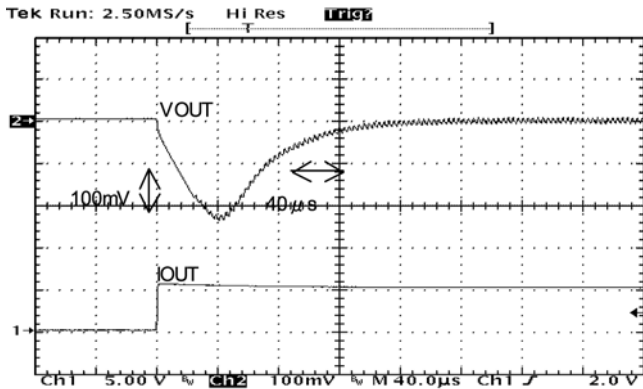
MODE: Low

FET: SUD30N03 (Vishay)

R<sub>SENSE</sub>: 33m $\Omega$

C<sub>L</sub>: 150 $\mu$ F (OS-CON, SANYO)

L: CDRH127/LD-7R4 (SUMIDA)



## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(20) Latch Protection Circuit Operating Waveform <MODE: High>

<Condition>

V<sub>IN</sub>: 5V

V<sub>OUT</sub>: 3.3V

MODE: High

FET: SUD30N03 (Vishay)

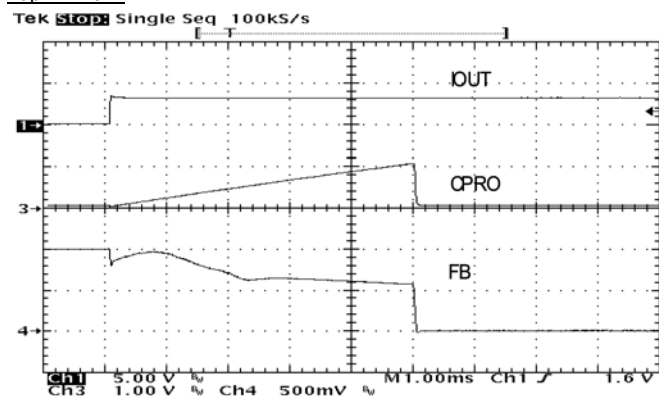
R<sub>SENSE</sub>: 33m $\Omega$

C<sub>PRO</sub>: ceramic 4700pF

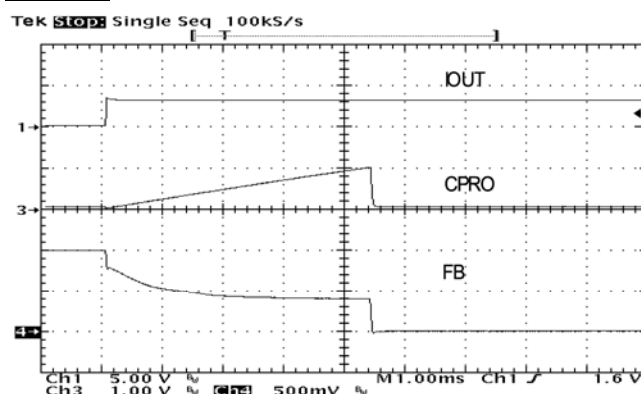
C<sub>L</sub>: 150 $\mu$ F (OS-CON, SANYO)

L: CDRH127/LD-7R4 (SUMIDA)

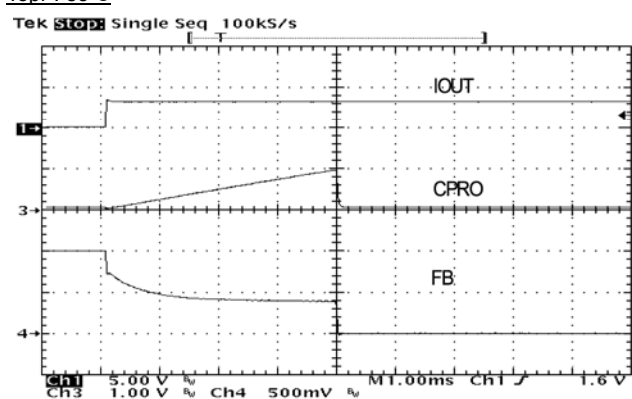
Topr: -40°C



Topr: 25°C



Topr: 85°C



## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### (21) Short-circuit Protection Circuit Operation Waveform

<Condition>

VIN: 5V

VOUT: 3.3V

MODE: High

FET: SUD30N03 (Vishay)

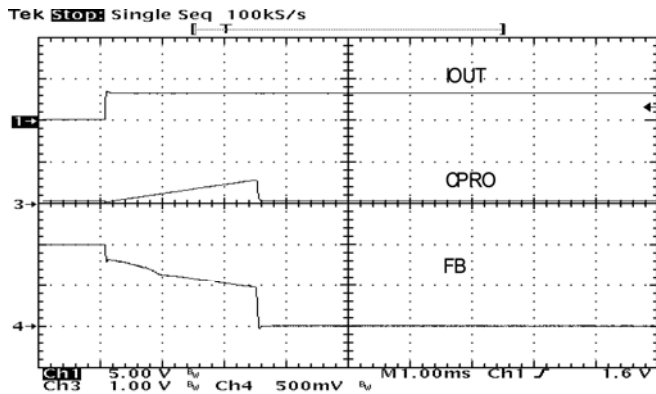
RSENSE: 33m $\Omega$

CPRO: ceramic 4700pF

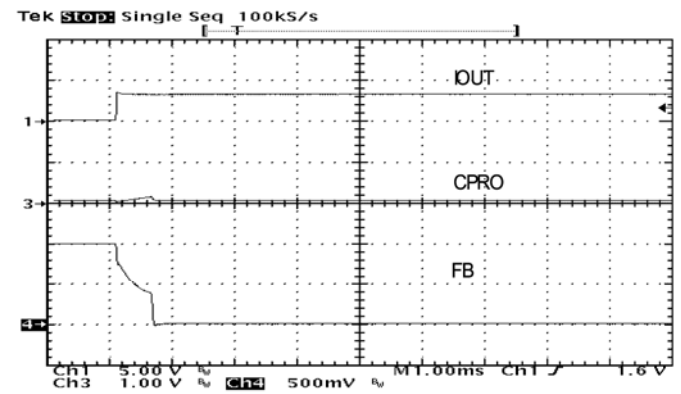
CL: 150 $\mu$ F (OS-CON, SANYO)

L: CDRH127/LD-7R4 (SUMIDA)

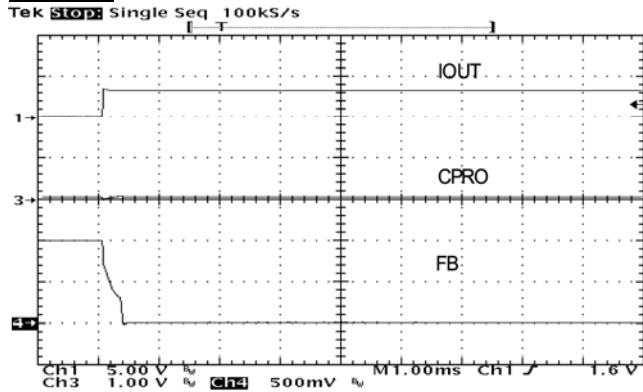
Topr: -40°C



Topr: 25°C



Topr: 85°C



### (22) Soft-start Circuit Operation Waveform

<Condition>

VIN: 5V

VOUT: 3.3V

IOUT: 100mA

MODE: High

Css: 4700pF

<Condition>

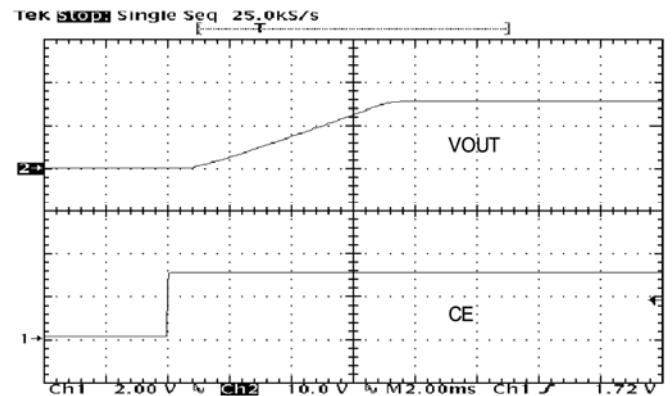
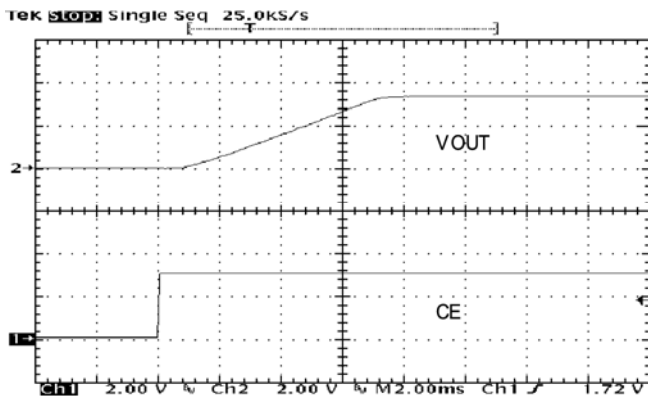
VIN: 20V

VOUT: 15V

IOUT: 100mA

MODE: High

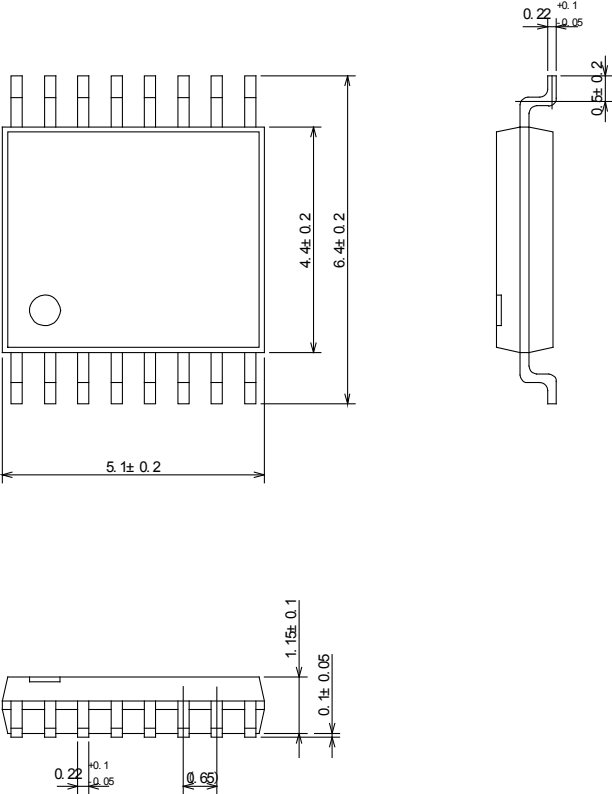
Css: 4700pF





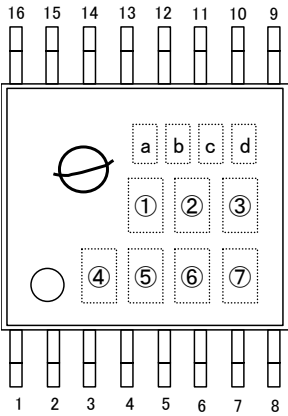
PACKAGING INFORMATION

TSSOP-16



MARKING RULE

TSSOP-16



TSSOP-16  
(TOP VIEW)

①②③④ represents product series

MARK				PRODUCT SERIES
①	②	③	④	
2	1	3	B	XC9213B103Vx

⑤⑥ represents standard voltage

MARK		VOLTAGE (V)	PRODUCT SERIES
⑤	⑥		
1	0	1.0	XC9213B103Vx

⑦ represents oscillation frequency

MARK	OSCILLATION FREQUENCY	PRODUCT SERIES
3	300kHz	XC9213B103Vx

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